

Mockingbird_CML (DIS)

Schematic Document

2019/12/09
REV: SC

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

Eletro-X

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

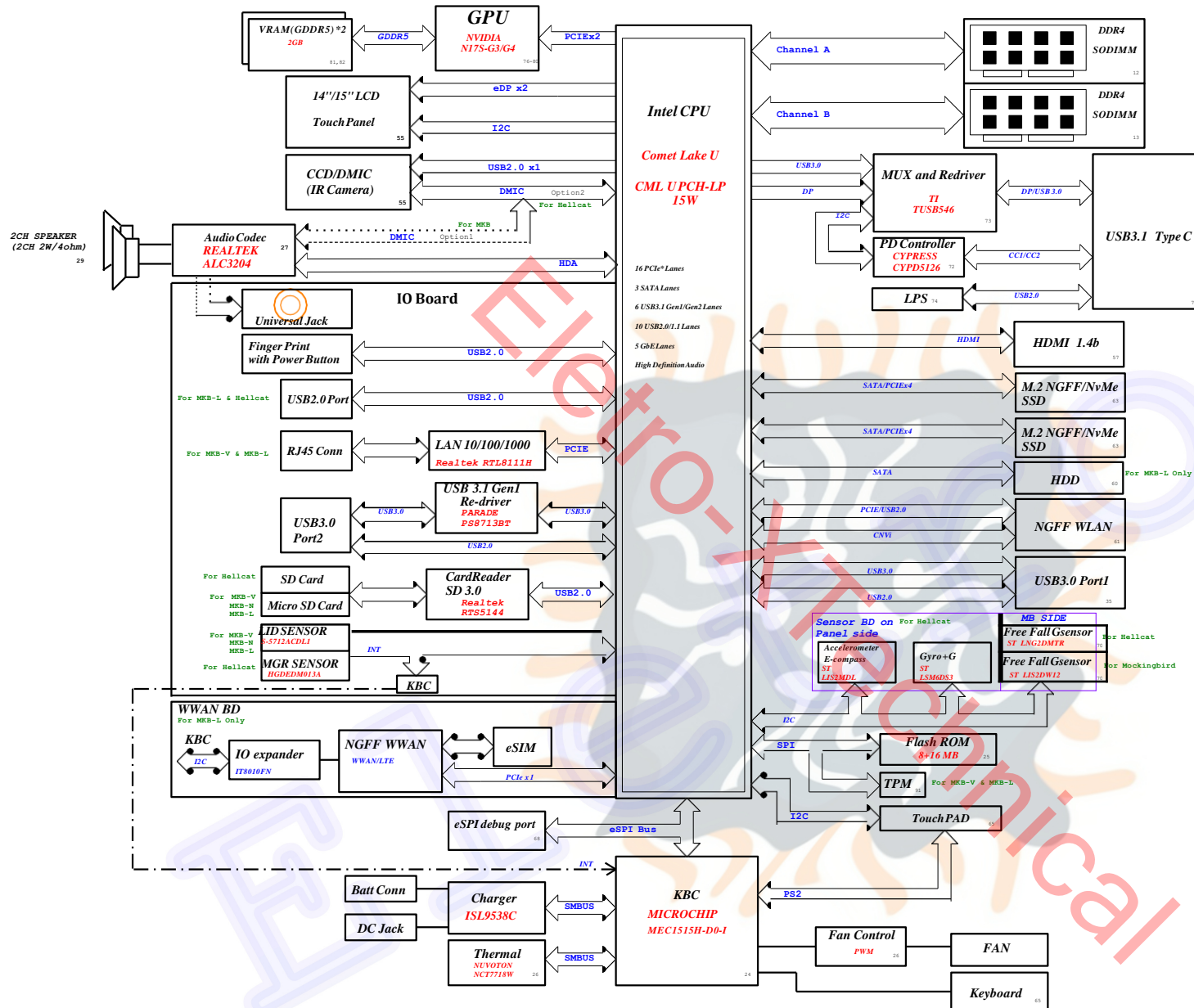
Mockingbird CML

Date: Monday, December 09, 2019

Sheet 1 of 1

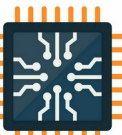


Mockingbird N/V/L/HellCat CML Block Diagram



Eleto-XTechnical

Eleto-XTechnical



PCH SMBus Block Diagram

KBC SMBus Block Diagram

Eletro-XTechnical

PCH

SMSC
MEC1404

TouchPad Conn.

Battery Conn.

HPA02224RGRR

HDMI CONN

©Com Design

DELL Wistron Corporation
2/F, 88, Sec. 1, Hsin-Tai Wu Rd.
Taichung City 404, Taiwan, R.O.C.

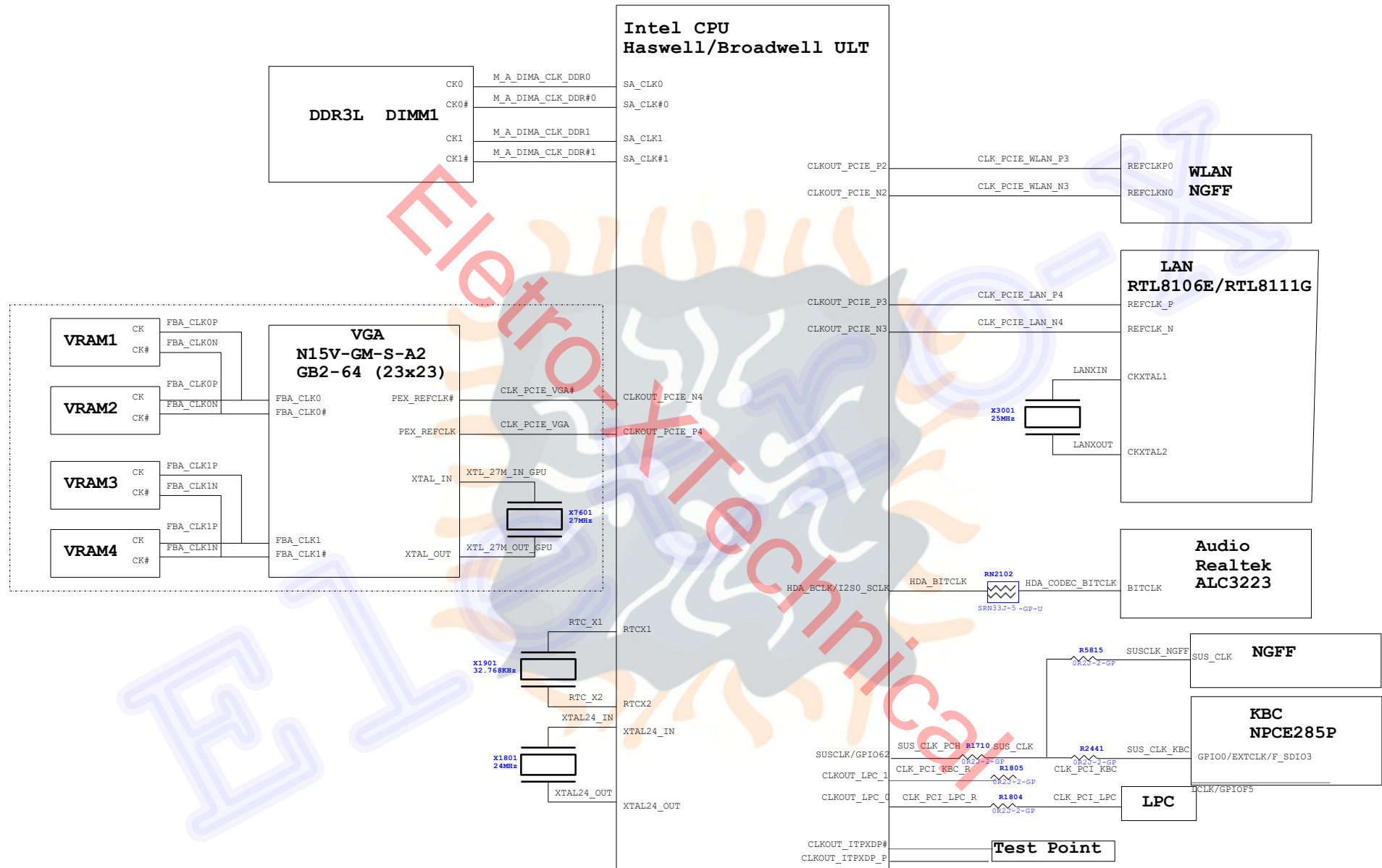
SMBUS Block Diagram
Mockingbird CML

Size: A2
Document Number:
Date: Moscow, December 09, 2019
Sheet 104 of 104

Eletro-X

CLK Block Diagram

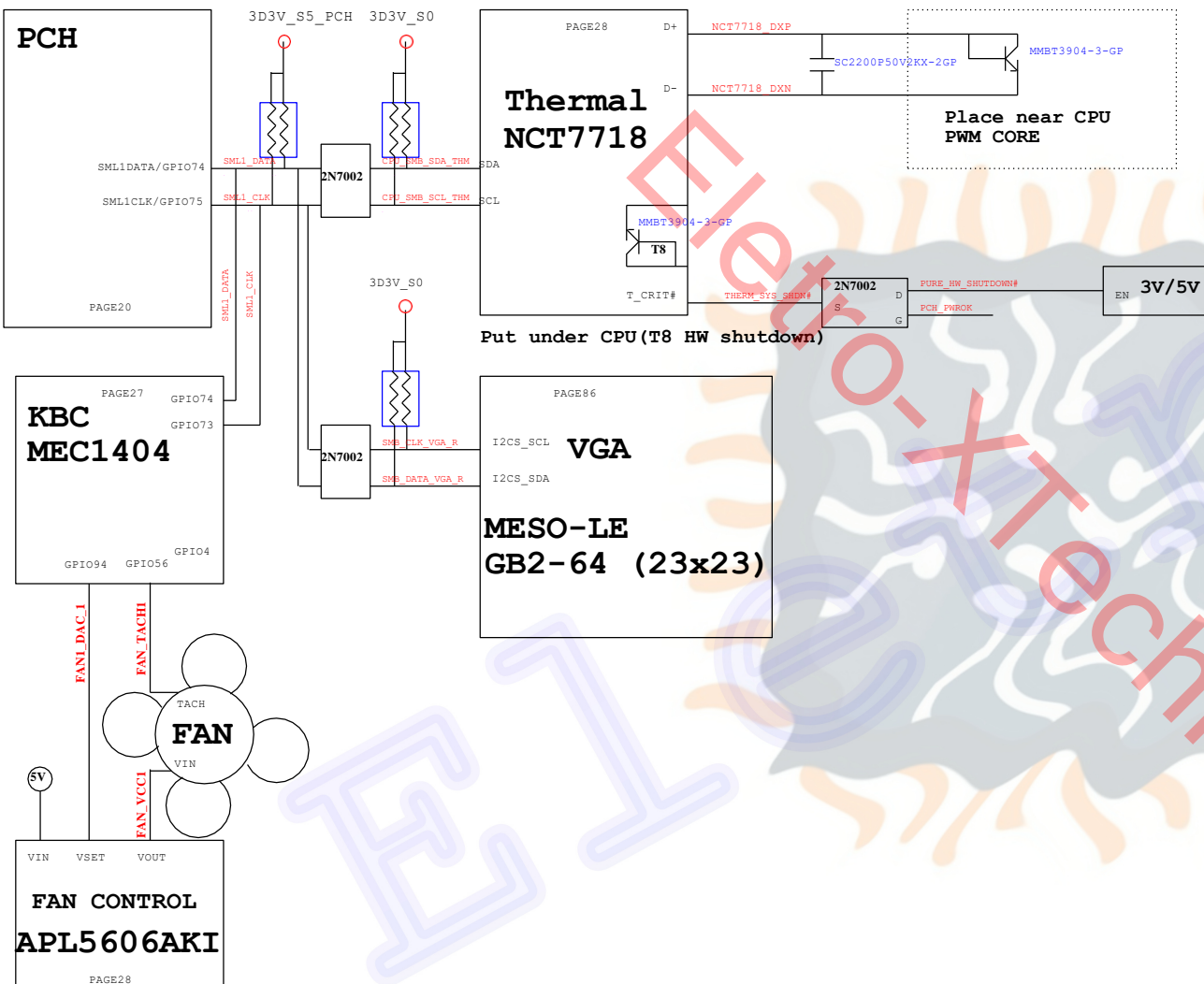
Eletro-XTechnical



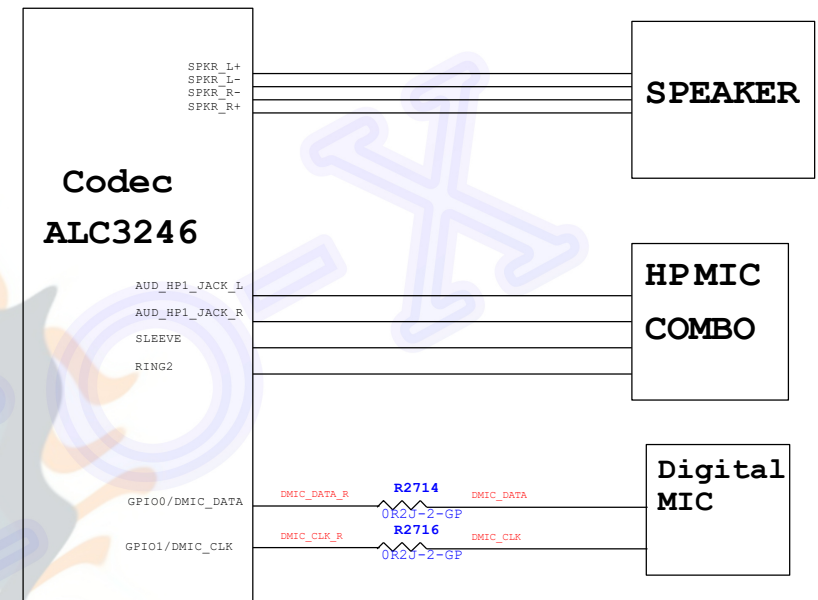
Eletro-XTechnical

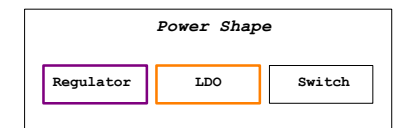
Eletro-X

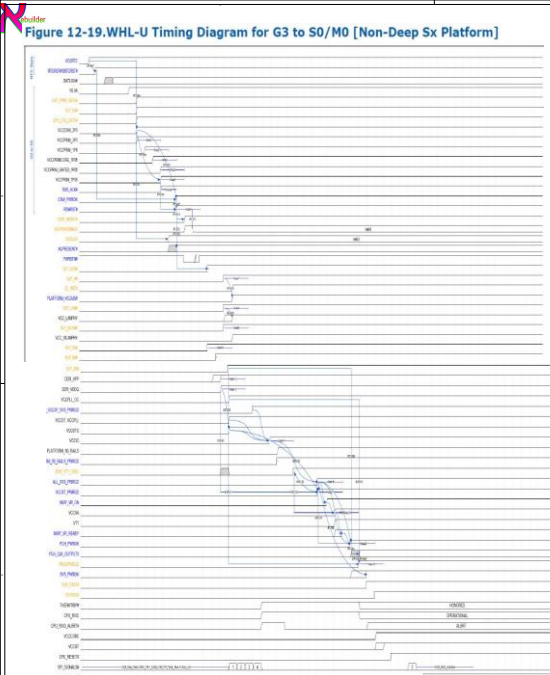
Thermal Block Diagram



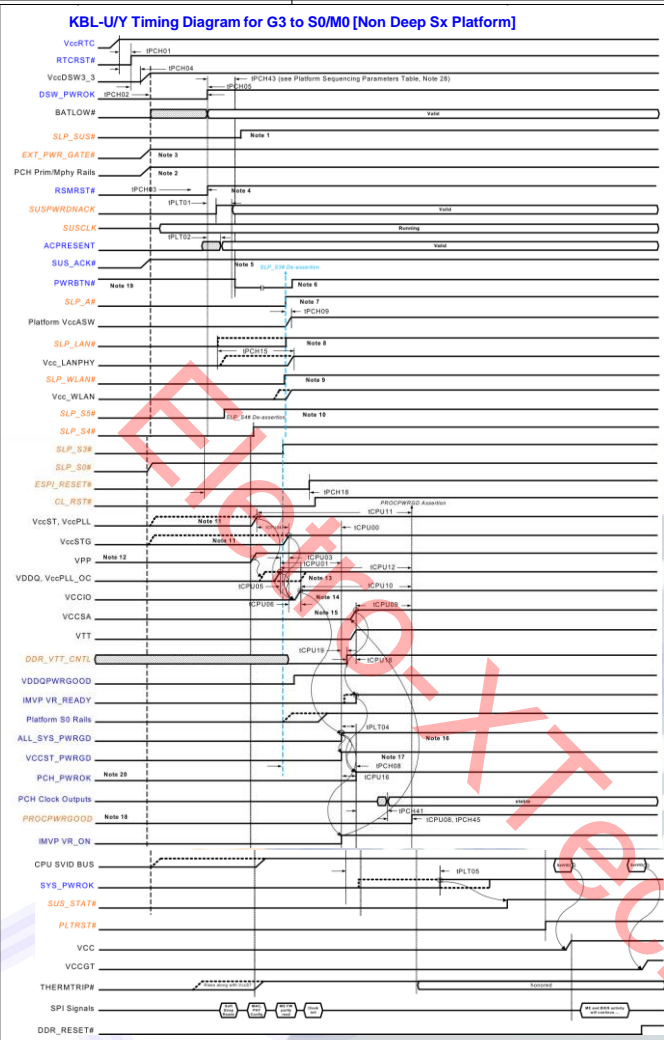
Audio Block Diagram



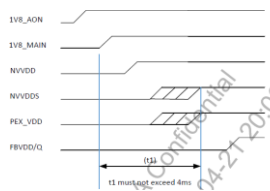




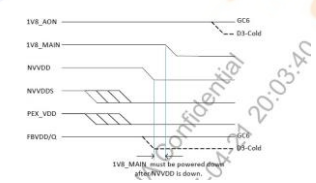
For DDR4 power sequence



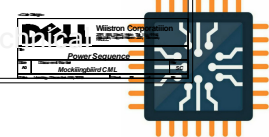
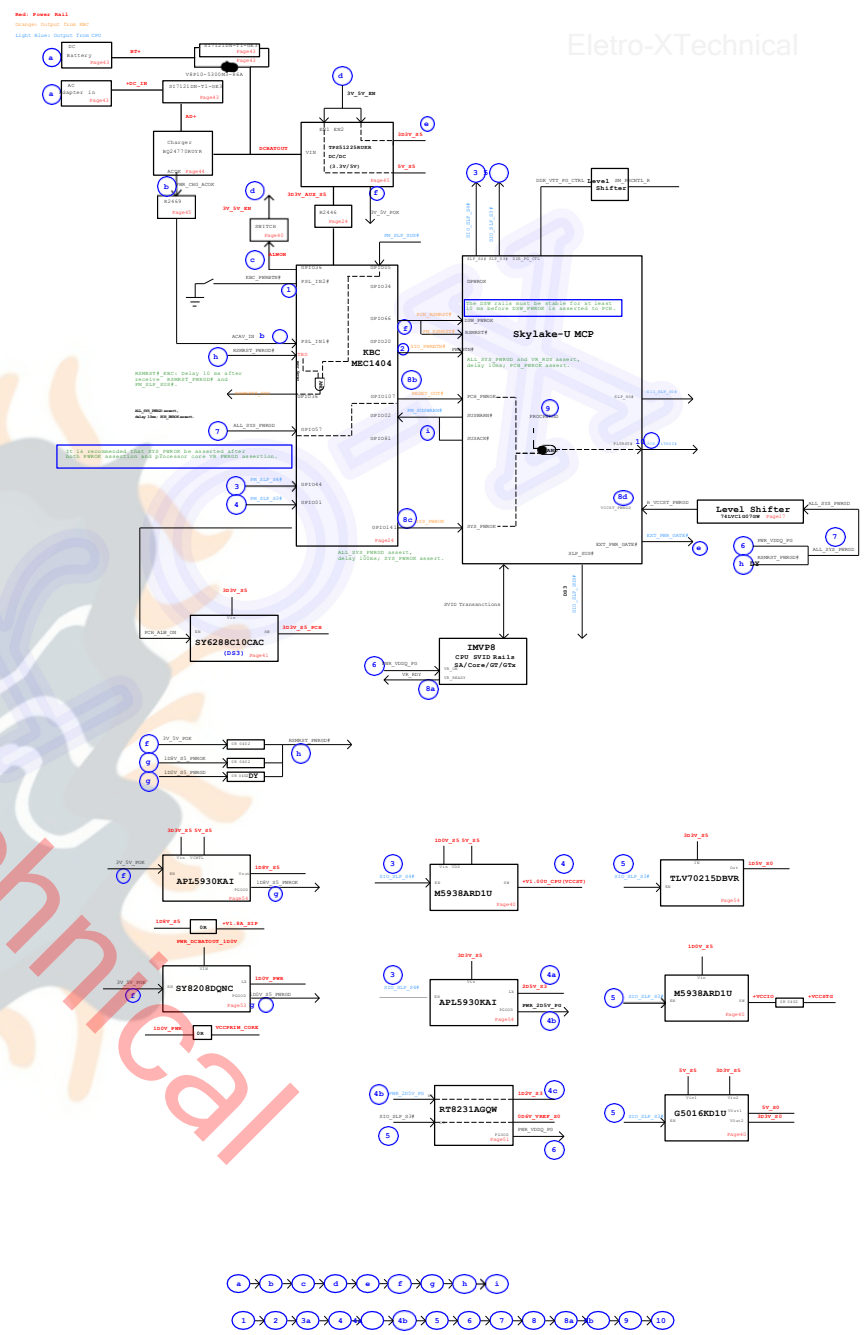
NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



SSID = CPU

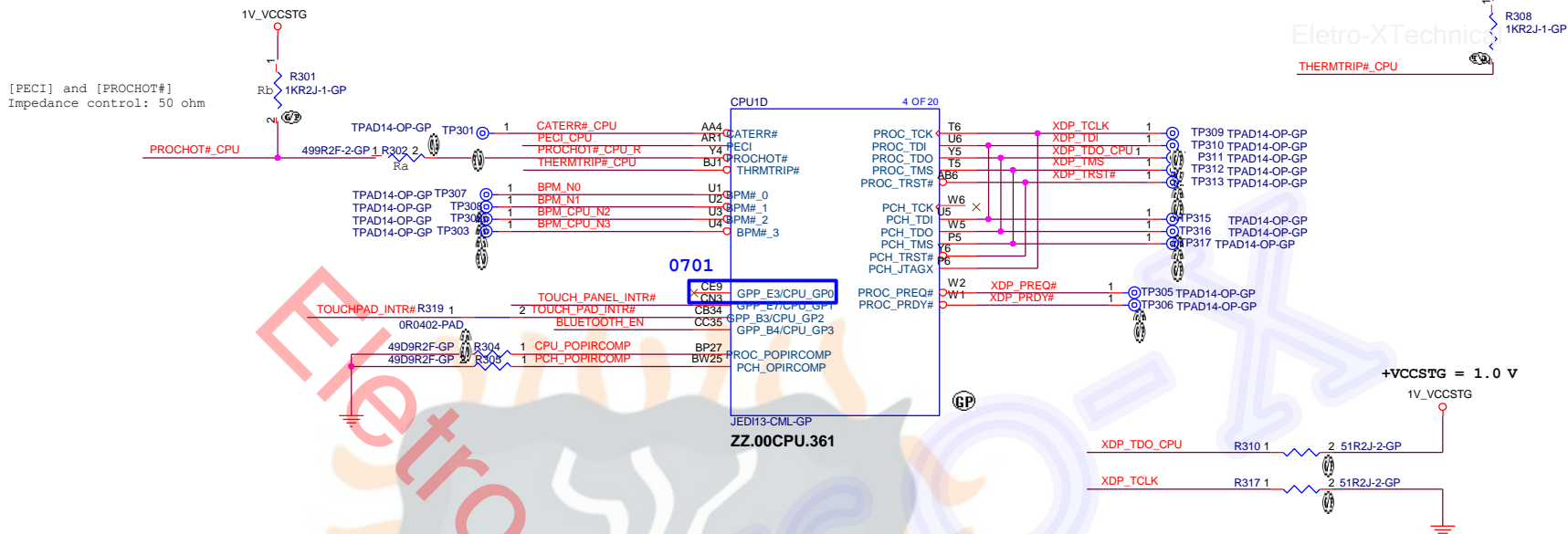
[24] PECO_CPU << >>—

[24,44,46] PROCHOT#_CPU << >>—

[55] TOUCH_PANEL_INTR# <<< —

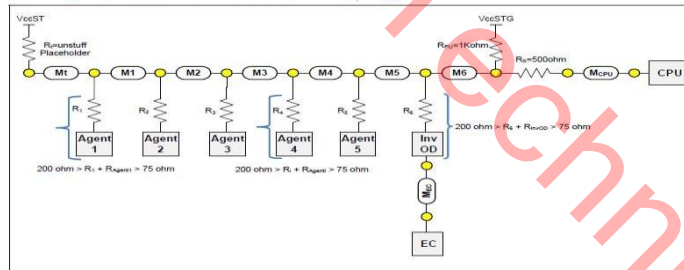
[24,65] TOUCHPAD_INTR# >>> —

[61] BLUETOOTH_EN <<< _____



(#543016) PROCHOT# Routing

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches



Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

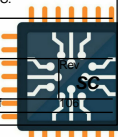
Title: **EL CPU (THML/JTAG)**

Size	Document Number
------	-----------------

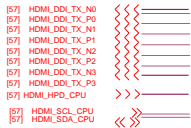
Mockingbird CML

Date: Monday, December 09, 2019

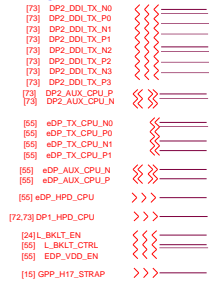
Sheet 3



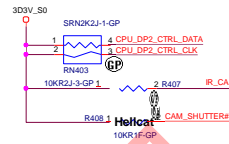
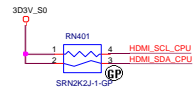
DP to HDMI2.0



DP for Type-C Mux



[55] IR_CAM_DET# >>>



Design Guideline: Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.

#543016 eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 $\Omega \pm 1\%$	Max = 100 mils

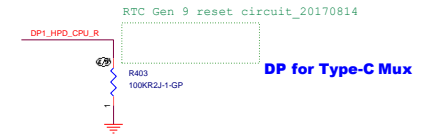
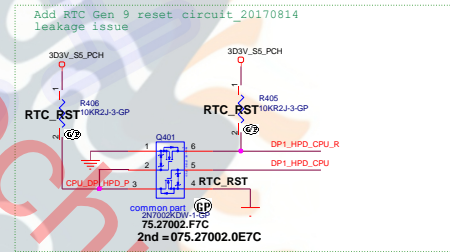
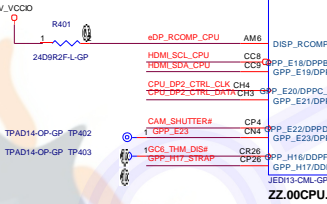
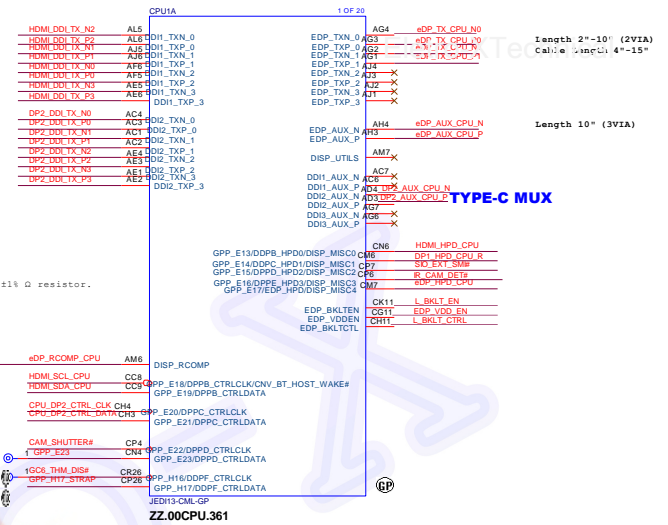
#543016 DDI Disabling and Termination Guidelines

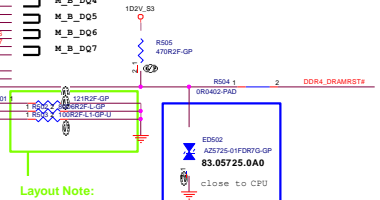
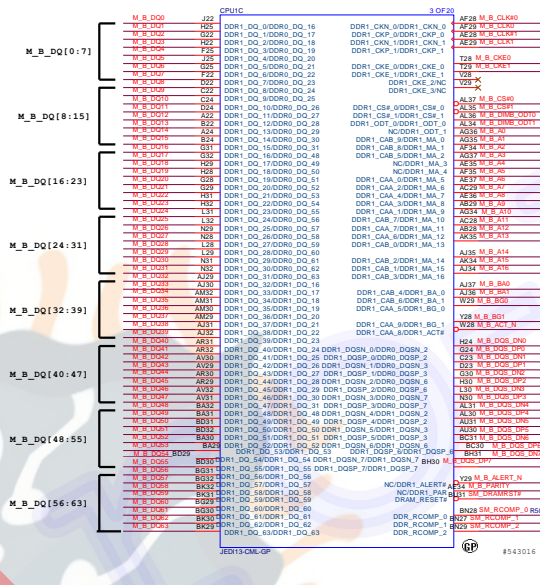
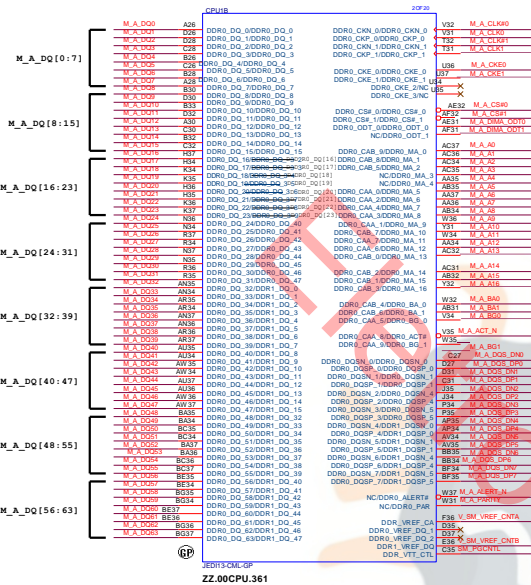
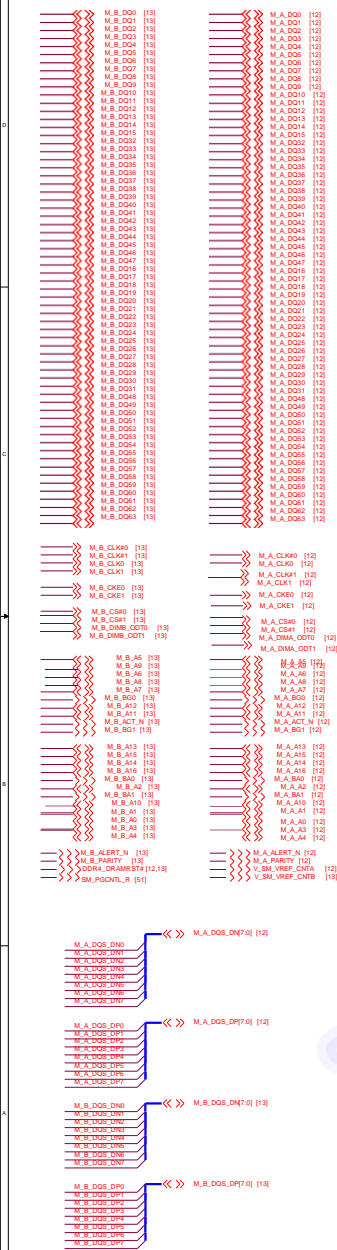
Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

1.650T Length 6.5" (3V1A)

DP to HDMI1.4b

DP for Type-C Mux





DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

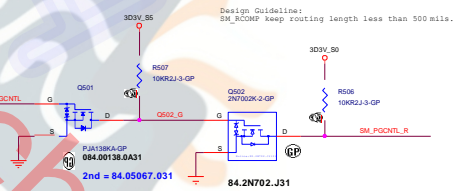
4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

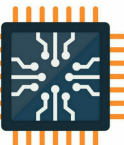
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

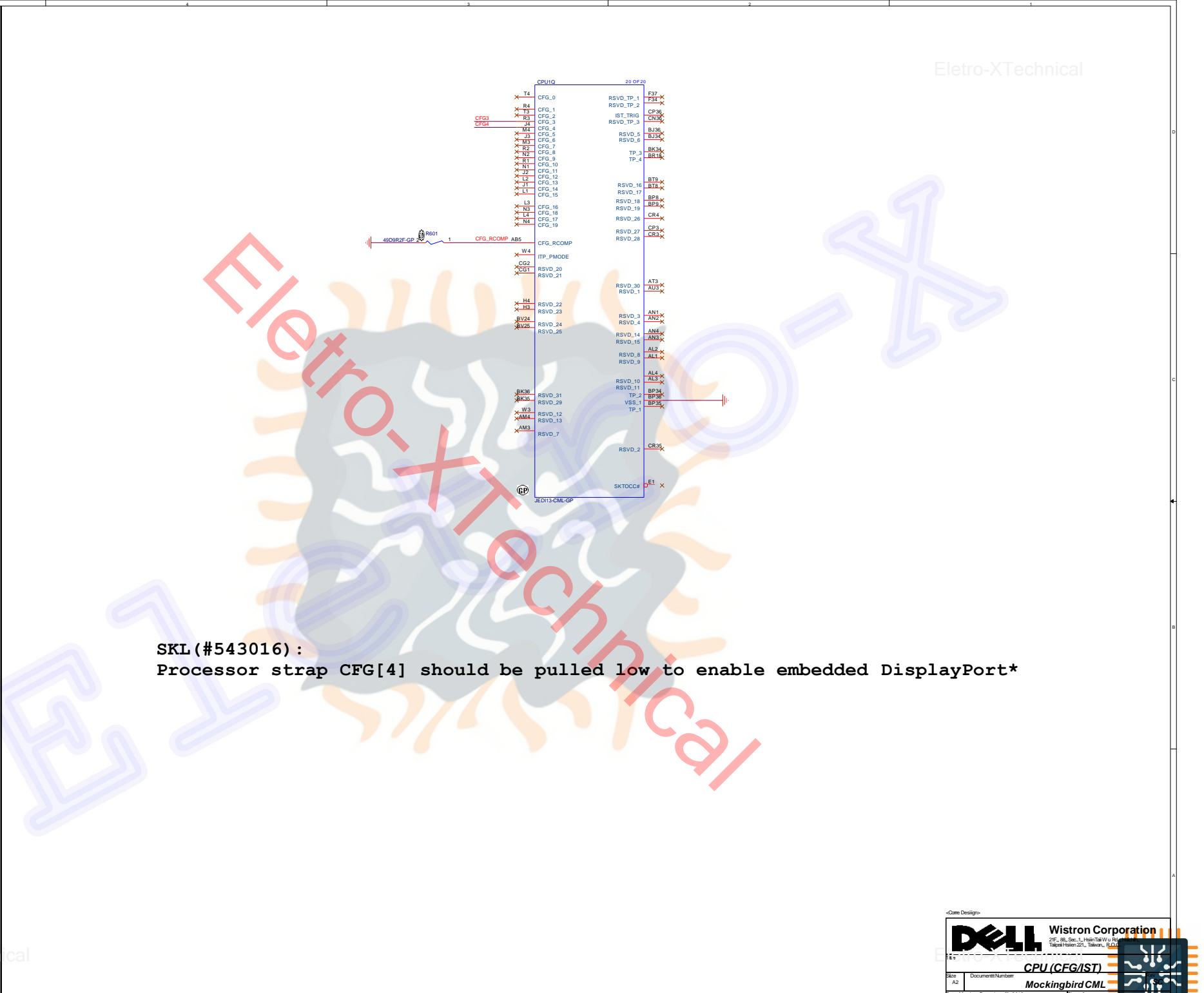
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



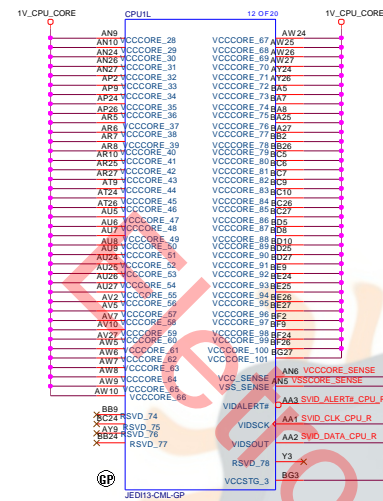
Layout Note:

0614 Layout HT





[46] VCCORE_SENSE <<<=====
[46] VSSCORE_SENSE <<<=====
[46] SVID_DATA_CPU <<<=====
[46] SVID_CLK_CPU <<<=====
[46] SVID_ALERTt_CPU <<<=====



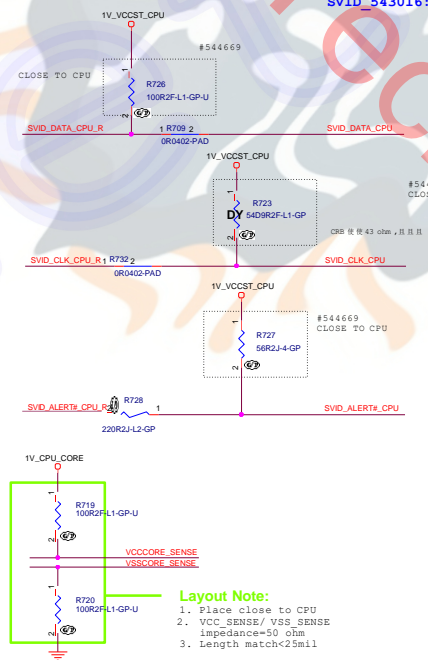
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (10.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID 543016:

SVID DATA

SVID CLOCK

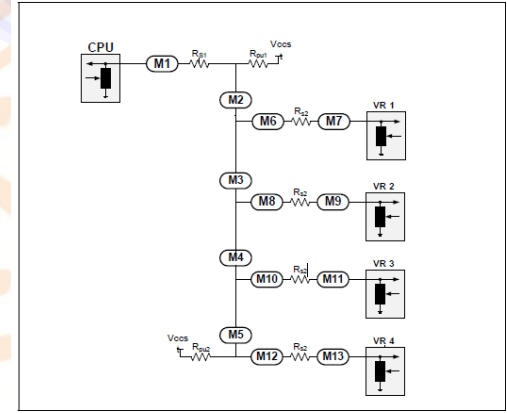
SVID ALERT



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE
impedance=50 ohm
3. Length match<25mil

Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13
Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#					
VIDSOUT platform resistors		Rpu1=1000, Rpu2=1000, Rsl=00, Rs2=100					
VIDSCK platform resistors		Rpu1=Empty, Rpu2=450, Rsl=00, Rs2=49.9Q					
VIDSALERT# platform resistors		Rpu1=560, Rpu2=Empty, Rsl=2200, Rs2=00					
Platform resistors tolerances		± 5%					
Route ordering		When routing at minimum spacing route Alert between Data and Clock					
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK		± 100mils					

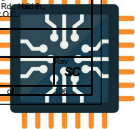
Routing Illustration for SVID Topology



Core Design

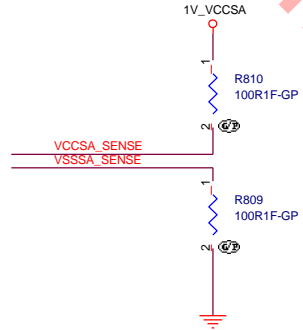
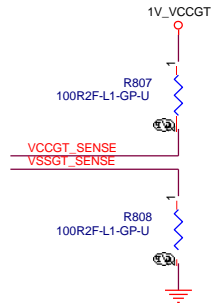
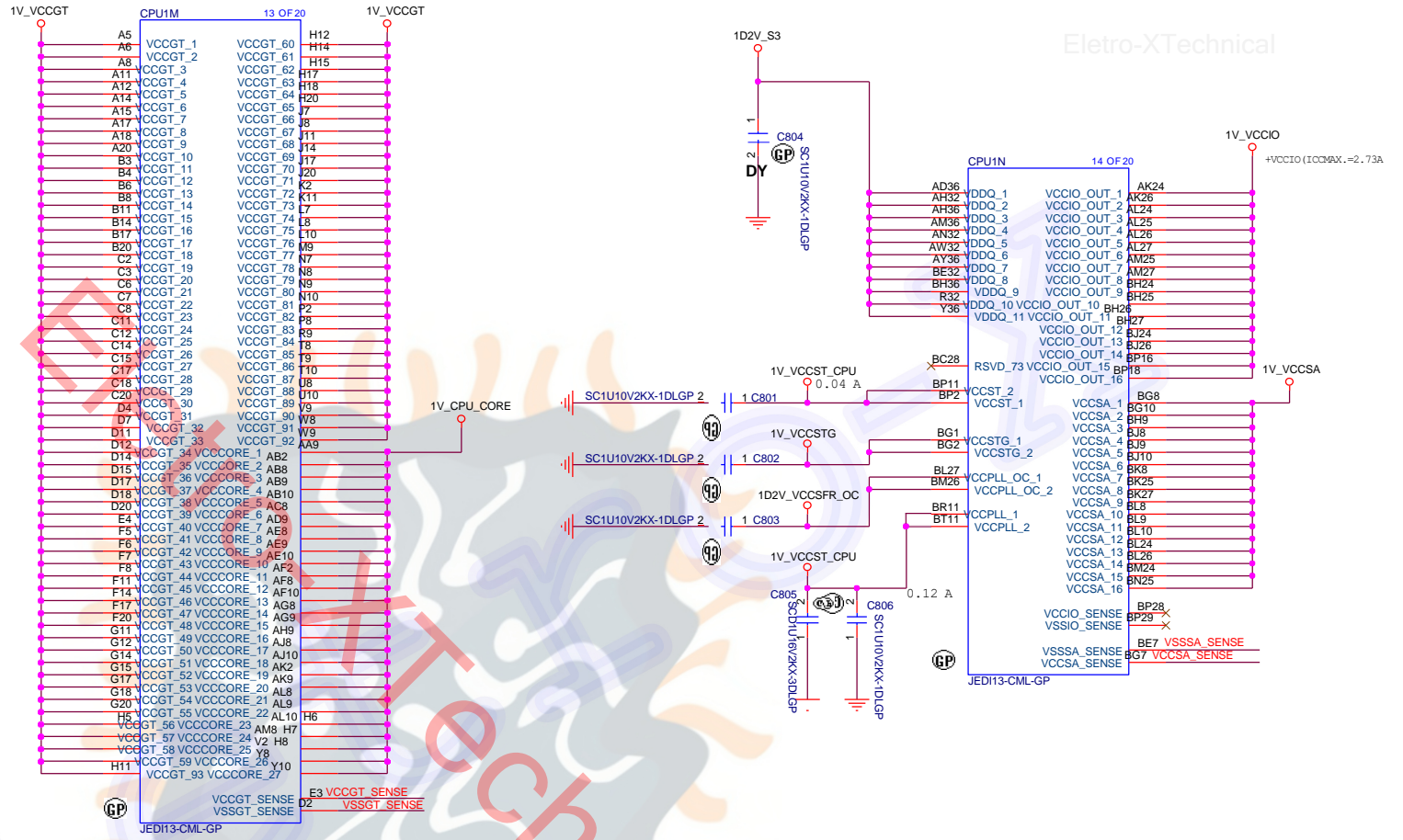


CPU (VCCIN/VID)	
Size	Document Number
A2	Mockingbird CML
Date	Monday, December 09, 2015
Sheet	7



[46] VSSSA_SENSE <<< —
 [46] VCCSA_SENSE <<< —
 [46] VCCGT_SENSE <<< —
 [46] VSSGT_SENSE <<< —

Pin Number	CFL-U43E	WHL E51 Netname	WHL E52 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



<Core Design>

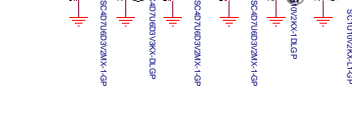
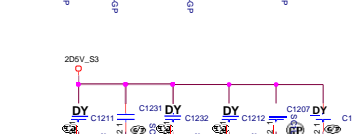
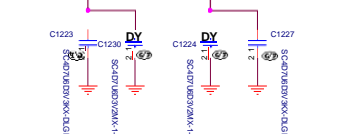
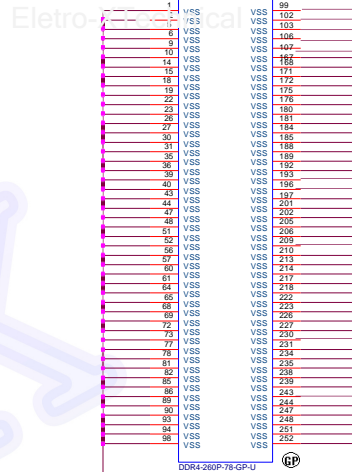
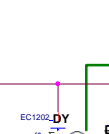
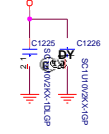
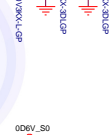
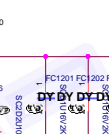
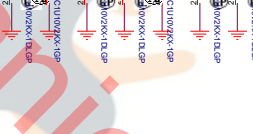
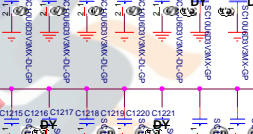
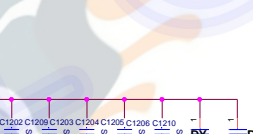
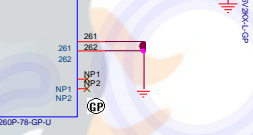
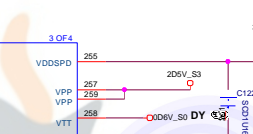
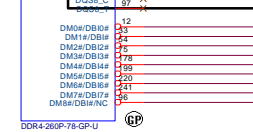
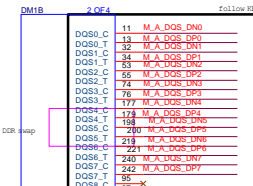
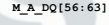
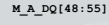
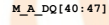
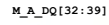
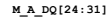
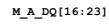
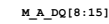
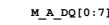
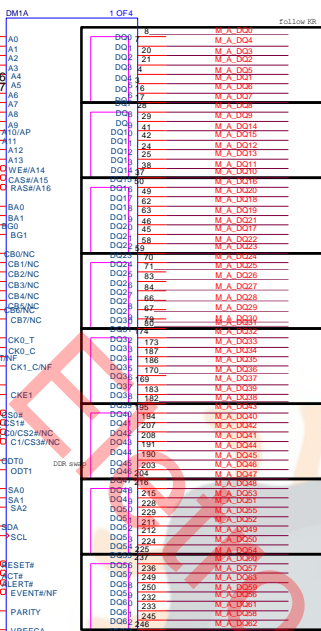
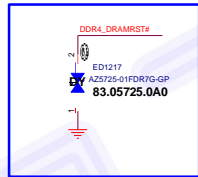
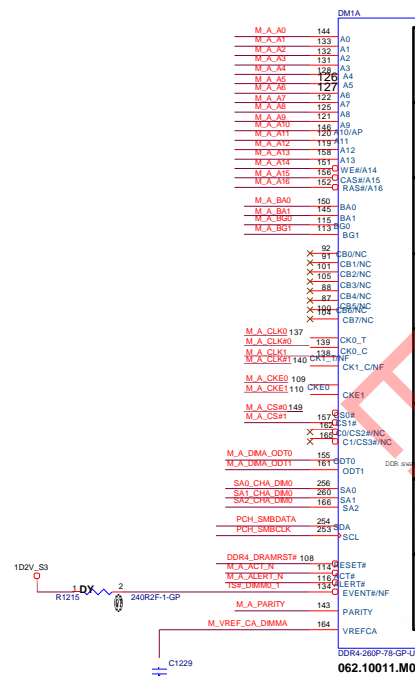
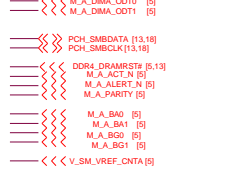
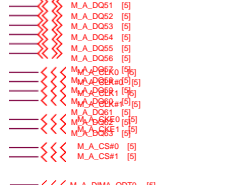
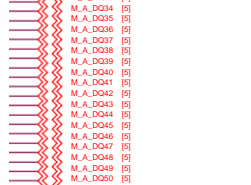
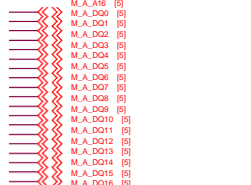
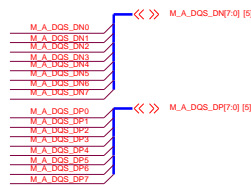
DELL Wistron Corporation
 21F, 88, Sec. 1, HsinTaiWu Rd., Hsichih,
 Taipei-Hsien 221, Taiwan, R.O.C.

Title: **CPU (VDDQ/VCC/VCCST/VCCSTG)**

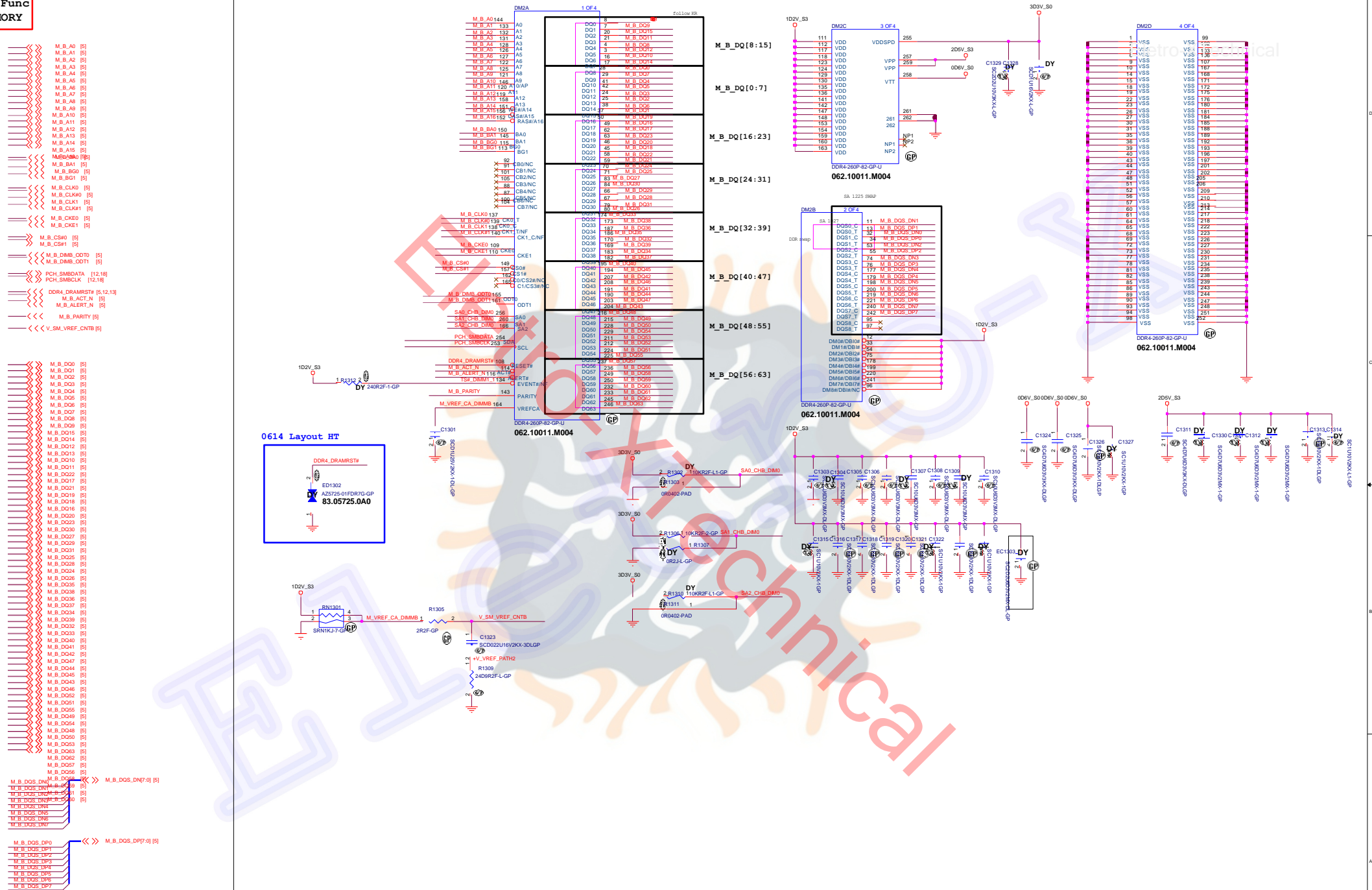
Size: A3 Document Number: **Mockingbird CML**

Date: Monday, December 09, 2019 Sheet 8 of 8

Main Func
= MEMORY



Main Func



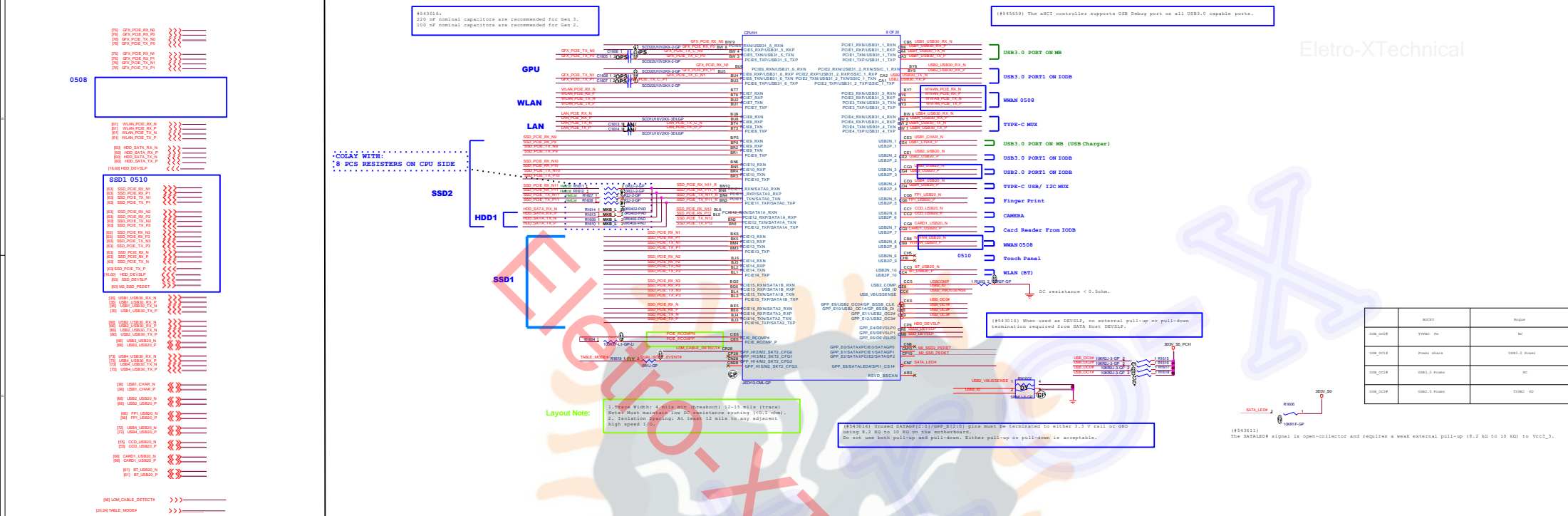


Table 24-2. PCI Express® Port Feature Details

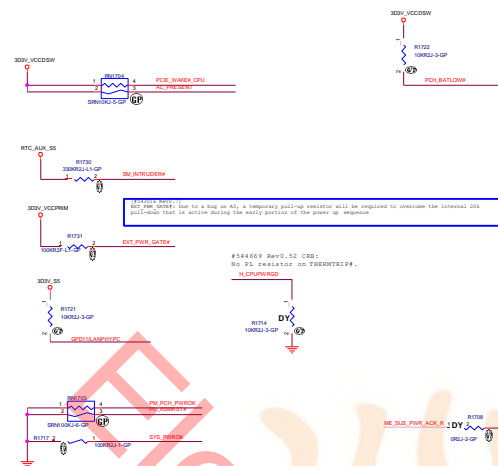
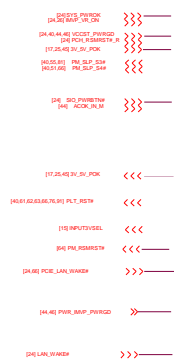
SKL	Max Device (Ports)	Max Lanes	PCIe® Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
				8b/10b	5000	0.50	1.00	2.00
				128b/130b	8000	1.00	2.00	3.94
Y	5	10	2	8b/10b	2500	0.25	0.50	1.00
				8b/10b	5000	0.50	1.00	2.00

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support

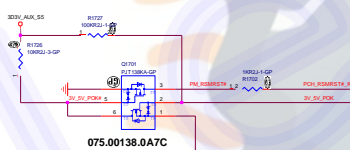
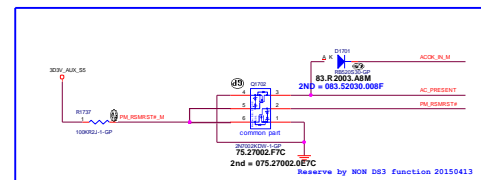
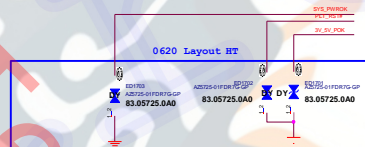
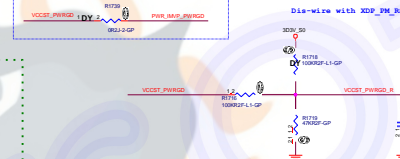
SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/Base-U	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	PCIe* Gen 1	PCIe* Gen 1	GbE 10G/PCIe*	GbE 10G/PCIe*	GbE 10G/PCIe*	PCIe* Gen 1	SATA 6Gbps/PCIe*	SATA 6Gbps/PCIe*	GbE 10G/PCIe*	GbE 10G/PCIe*	PCIe* Gen 1	PCIe* Gen 1
Premium-U	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	GbE 10G/PCIe*	GbE 10G/PCIe*	GbE 10G/PCIe*	PCIe* Gen 1	PCIe*/SATA 6Gbps	PCIe*/SATA 6Gbps	GbE 10G/PCIe*	GbE 10G/PCIe*	PCIe*/SATA 6Gbps	PCIe*/SATA 6Gbps
Premium-Y	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	GbE 10G/PCIe*	GbE 10G/PCIe*	GbE 10G/PCIe*	PCIe* Gen 1	PCIe*/SATA 6Gbps	PCIe*/SATA 6Gbps	GbE 10G/PCIe*	GbE 10G/PCIe*	Not Available	Not Available

PCH-LP	PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	2x4	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23	RP25	RP27	RP29
	1x4 LR	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23	RP25	RP27	RP29
	2x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23	RP25	RP27	RP29
	2x12	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15





AOZ Power switch, P/N: 074.01334.0093
Low Rds(on) = 5m Ohm
Turn on rise time = 10us



External Pull-up requirement for SLP_S0# and EXT_PWR_GATE# signal pins

SLP_S0# and EXT_PWR_GATE# signal pins require External Pull-up and the details are given below:

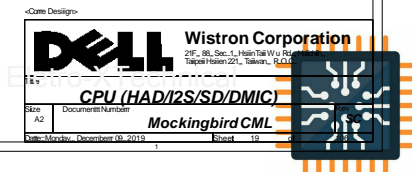
Signal Name	Pull-up Resistor Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
EXT_PWR_GATE#	100K	75K	Pull-up resistor is required.
SLP_S0#	100K	75K	Pull-up resistor is required. If a device is not using SLP_S0# to interface the controller.

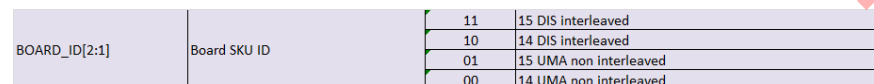
BATLOW#:
Pull-up required even if not implemented.



```
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
```


Eletro-X





	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB 可以動
Tablet Mode	don't care	0	KB 鎖住
ClamShell Mode	0	1	KB 鎖住

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

0614 Layout HT 3D3V_S5

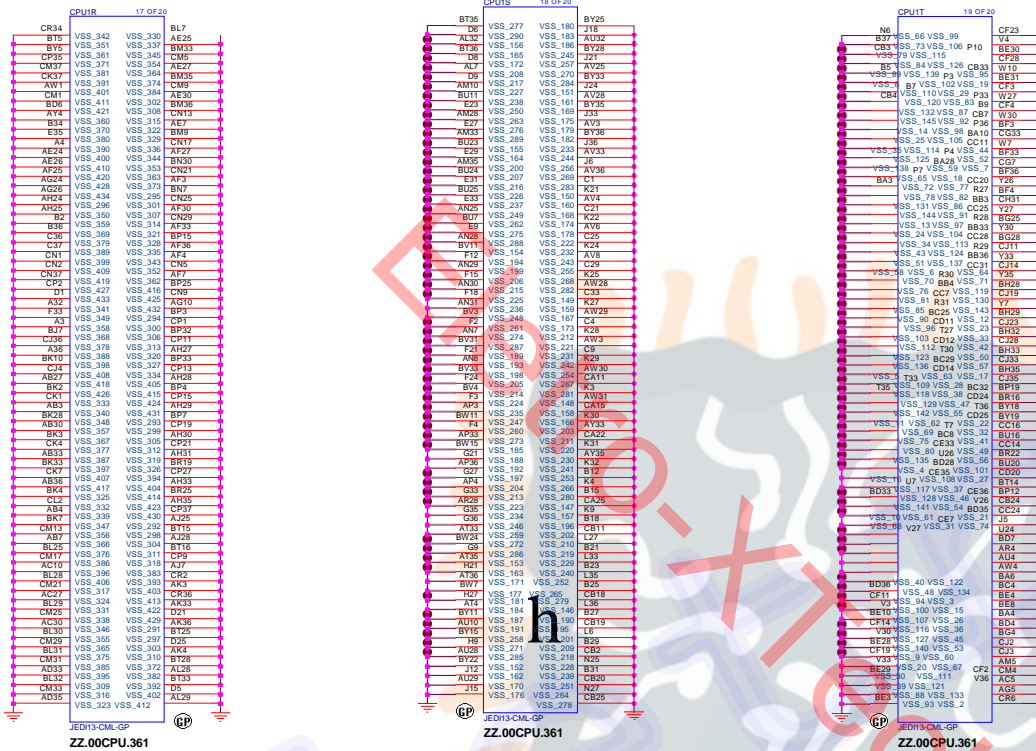


I. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

[illegible]

Voltage Supply	Area	PCB Pins sharing power rail	Value	Size	Quantity	Placement type (Jumper / EJE)	Place capacitor(s) near load(s)
V3.3A	VCCPRIM_3P3	C822, C823, C823, C823, C822, C823, C829, BV23, C813, C816	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.5A	VCCSP1	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCCHDA	BT20	-	-	-	-	-
V3.305 W	VCCDSW_G90	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1	E	BR23
PCB Internal VDD	VCCDSW_IP05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_IP24	BV23, CA23, CP25, BV24, CA24	4.7uF	0402	1	E	CP25

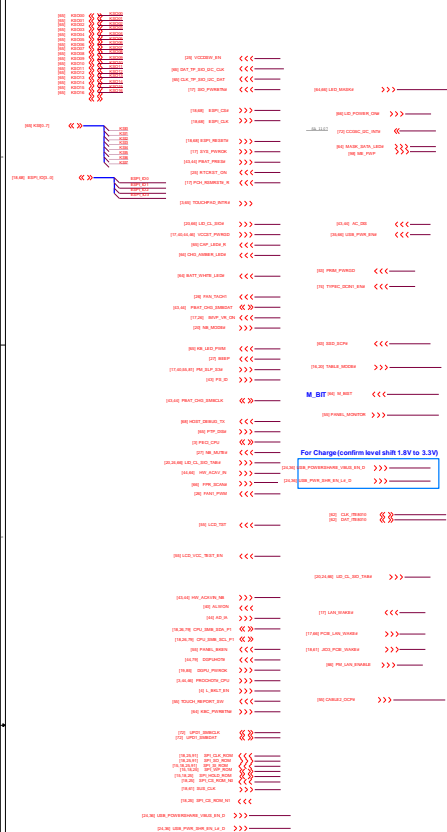
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of Run/way, and (E)edge decoupling capacitor placement, refer to "Loop Inductance Reduction and Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement.
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>



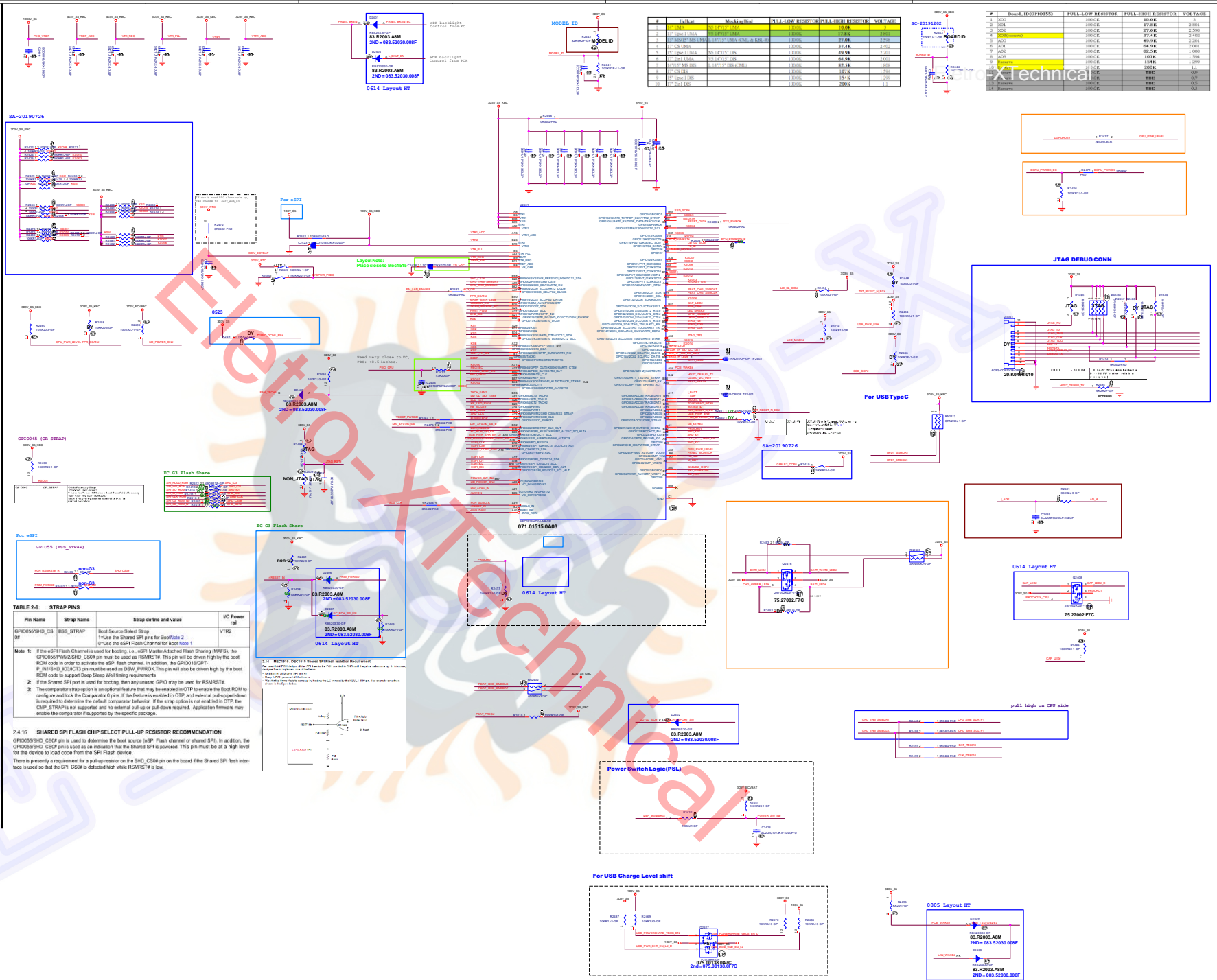
Pin Name	Strap Name	Strap define and value	I/O Power
----------	------------	------------------------	-----------

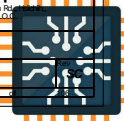
Device Name		Device Version		Part
GP0050SHD_C3	BIS_STRAP	Boot Secure Status Bit		Y1K92
- Enable the Shared SPI port for Boot/Note 2 - C-Use the eSPI Flash Memory for Boot/Note 1				
Note 1: <ul style="list-style-type: none"> If the eSPI Flash Memory is used for booting, i.e., after Master Attached Boot (MAB), the GP0050SHD_C3 must be set to 1 to enable the Shared SPI port. If the Shared SPI port is the boot ROM code in order to activate the eSPI Flash Memory, this can be the option GP0050SHD_C3_P1_SHD_ROM_CODE to be used as BIOS_PWNK0. This pin will also be driven high by the boot ROM code in support device. If the Shared SPI port is used for booting, then any unused GP0050SHD_C3 pin must be used for RSMRST#. 				
Note 2: <ul style="list-style-type: none"> The comparator input port is an optional feature that may be enabled in OTP to enable the Boot ROM to check the lock of the comparator. The comparator is not supported in the eSPI Flash Memory. It is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down needed. Application firmware is not required. 				

2.4 16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/6/7/8/9/CS0# pin is used to determine the boot source (aSPI Flash channel or shared SPI). In addition, the GPIO055/6/7/8/9/CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSNRST# is low.



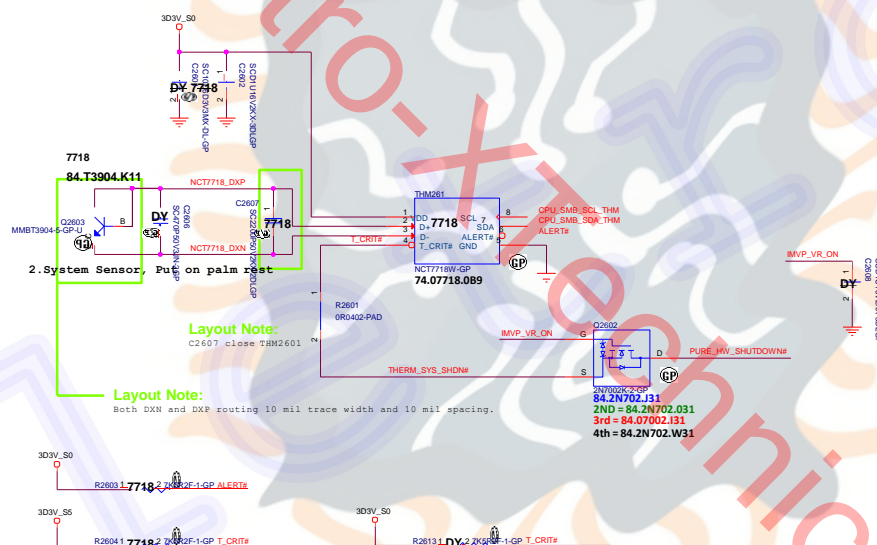
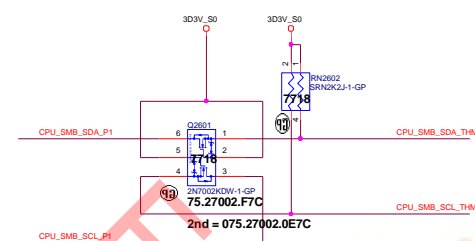


Layout Note:
Signal Routing Guideline:
Trace width = 15mil

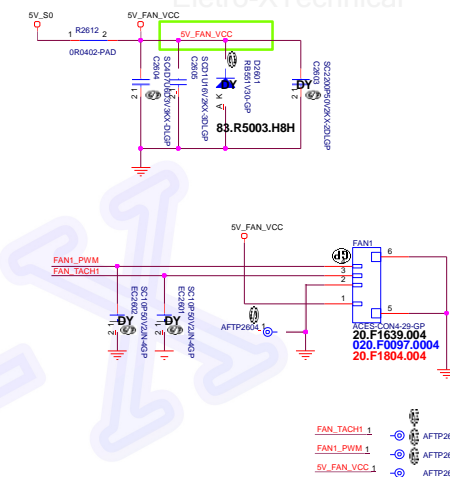
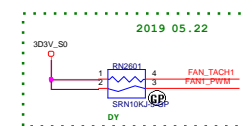
[18,24,78] CPU_SMB_SDA_P1 << >>
[18,24,78] CPU_SMB_SCL_P1 << >>

[17,24] MVP_VR_ON >>> >>>
[40] PURE_HV_SHUTDOWN# <<< <<<

[24] FAN1_PWM >>> >>>
[24] FAN1_TACH1 <<< <<<



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



FAN1_TACH1 1 AFTP2601
FAN1_PWM 1 AFTP2602
5V_FAN_VCC 1 AFTP2603

```
[19] HDA_SDIN0_CPU      <<< _____
[19]HDA_SDOUT_CODEC      >>> _____
[19] HDA_SYNC_CODEC      >>> _____
[19] HDA_BITCLK_CODEC    >>> _____
```

[29] AUD_SPK_R+ <<< _____

[29] AUD_SPK_R- <<< _____

[29] AUD_SPK_L+ <<< _____

[29] AUD_SPK_L- <<< _____

```

[24] NB_Mute#          >>> _____
[15,19] SPKR           >>> _____
[24] BEEP              >>> _____
[66] AUD_SENSE         >>> _____

[23] LINE1_VREF0       <<< _____
[23] MIC2_VREF0       <<< _____

[29] AUD_HP1_JACK_L    <<< _____
[29] AUD_HP1_JACK_R    <<< _____

[29] LINE1_L           >>> _____
[29] LINE1_R           >>> _____

```

[29,66] AUD_SLEEVE <<< _____

[29,66] AUD_RING <<< _____

55] DMIC_SCL_CODEC <<< _____

55] DMIC_SDA_CODEC <<< _____

[81] 1D8V_EN# >>> _____

Azalia I/F EMI

HDA, SDOUT CODEC
HDA, IITC15 CODEC

DY EC2709

2 1

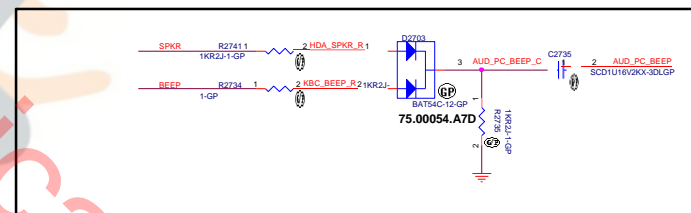
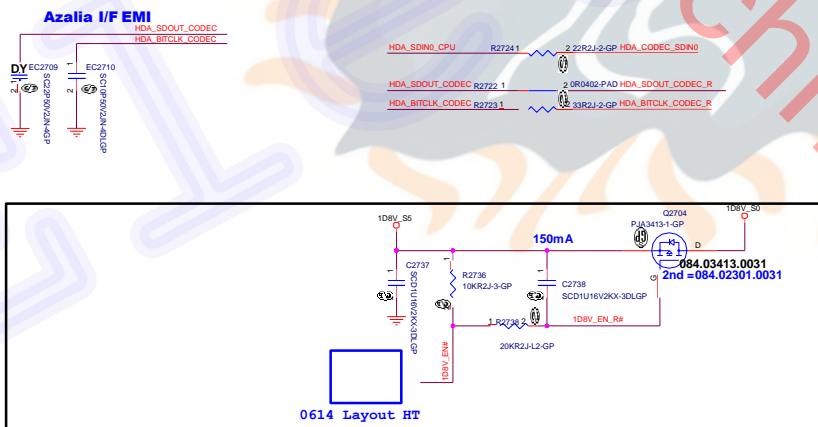
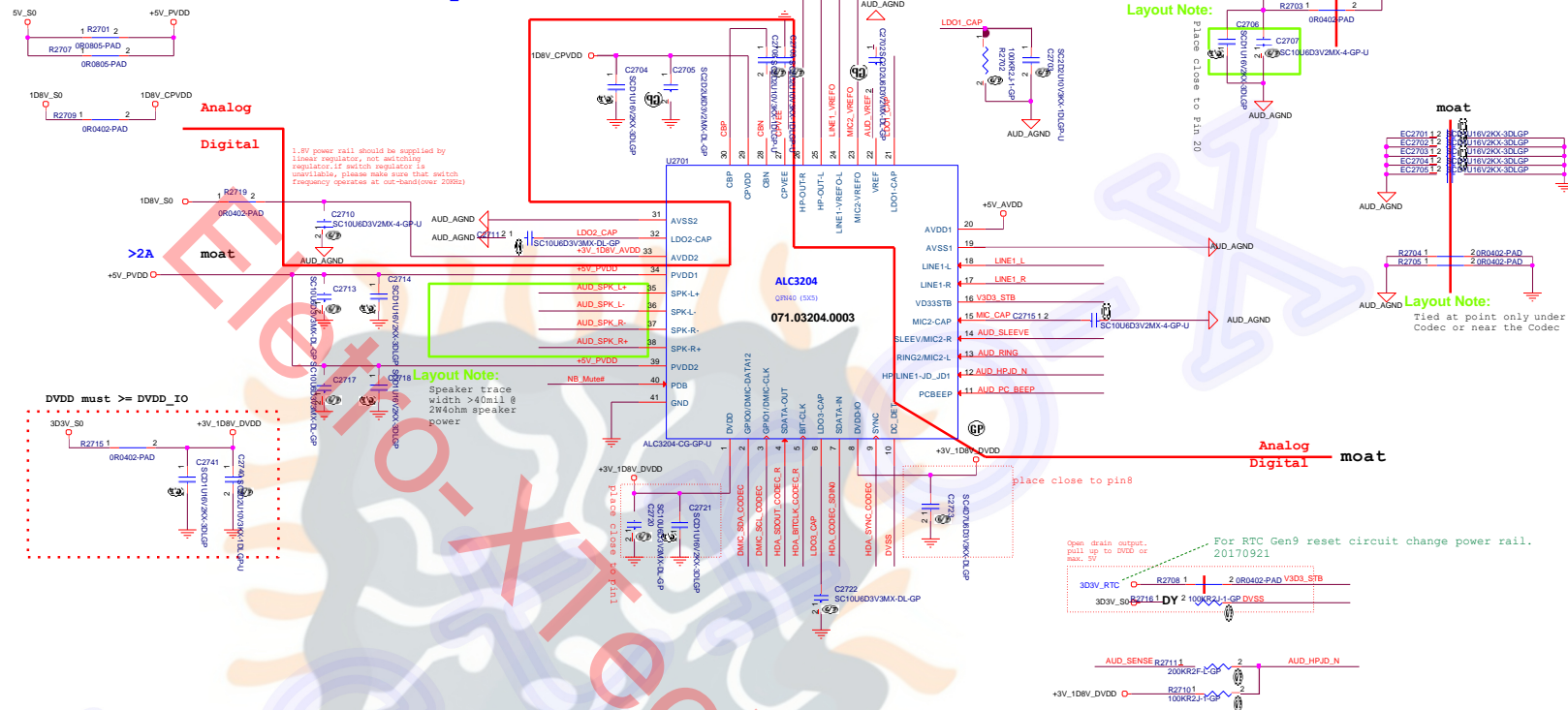
EC2710

2 1

N70705-4P

N70705-6J3P

Audio Codec Chip ALC3204



Main Func = USB3.0 Port1

[24,66] USB_PWR_EN# <<< _____

[16,36] USB_OC2# <<< _____

[36] USB1_USB20_N << >> _____

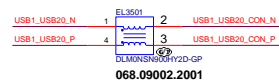
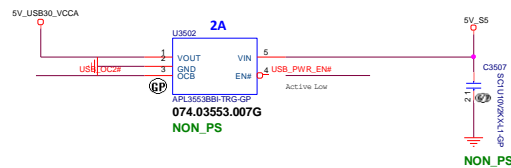
[36] USB1_USB20_P << >> _____

[16] USB1_USB30_TX_N >>> _____

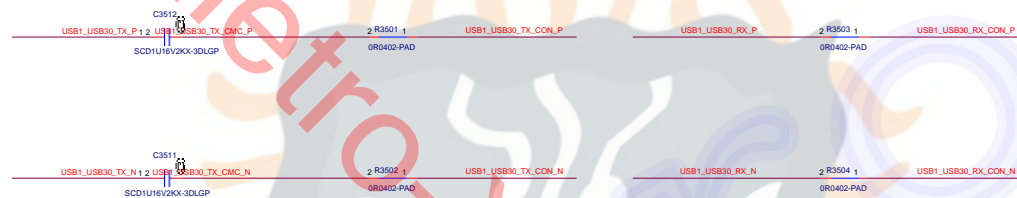
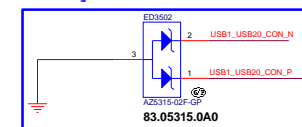
[16] USB1_USB30_TX_P >>> _____

[16] USB1_USB30_RX_N >>> _____

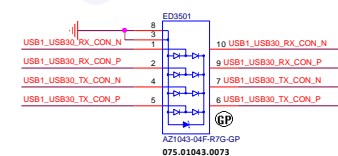
[16] USB1_USB30_RX_P >>> _____



0614 Layout HT

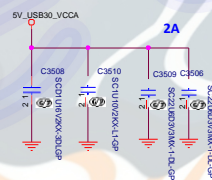


Stuff for ESD R2 spec

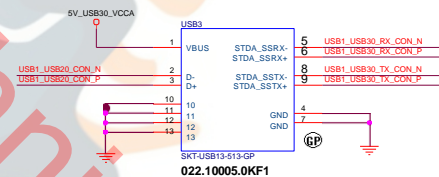


USB3.0 Port 1

Layout Note: Close USB3



USB3.0 Port1



Main Func = USB3.0 Port2

0513



Eletro-XTechnical

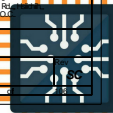
Eletro-X

<Came Design>

Wistron Corporation
2/F, 88, Sec. 1, Hsin-Tai Wu Rd.
Taichung, Taiwan 40401, Taiwan

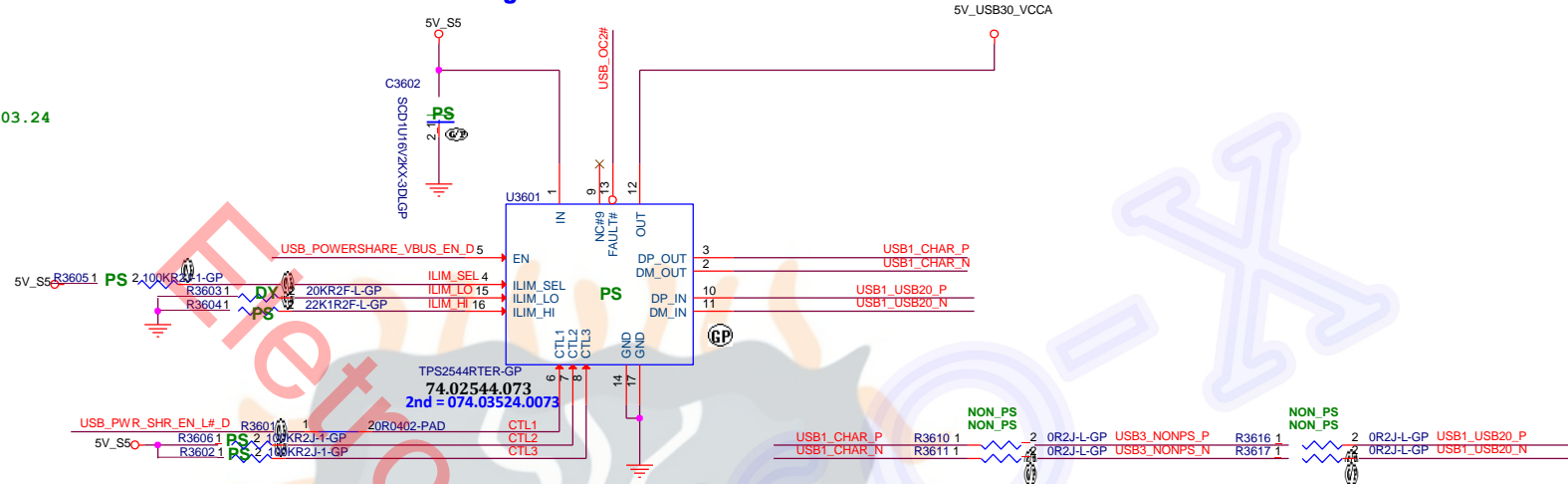
Mockingbird CML

Size: A2
Document Number: Mockingbird CML
Date: Monday, December 18, 2018
Rev: 35



2018.03.24

USB Charger Port1



[16] USB1_CHAR_P <<<
[16] USB1_CHAR_N <<<

[35] USB1_USB20_N <<<
[35] USB1_USB20_P <<<

Device Control Pins				
	CTL1 (EC control)		CTL3	
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS_DP} (mA) = \frac{50,500}{(R_{ILIM_XX} (k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

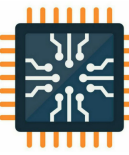
[24] USB_POWERSHARE_VBUS_EN_D >>>

[24] USB_PWR_SHR_EN_L#_D >>>

[16,35] USB_OC2# <<<

<Core Design>

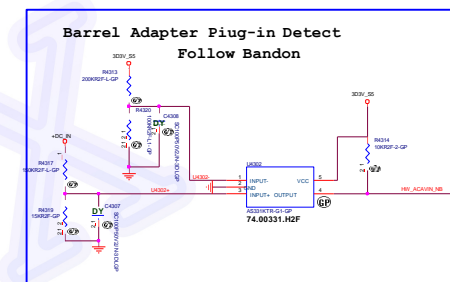
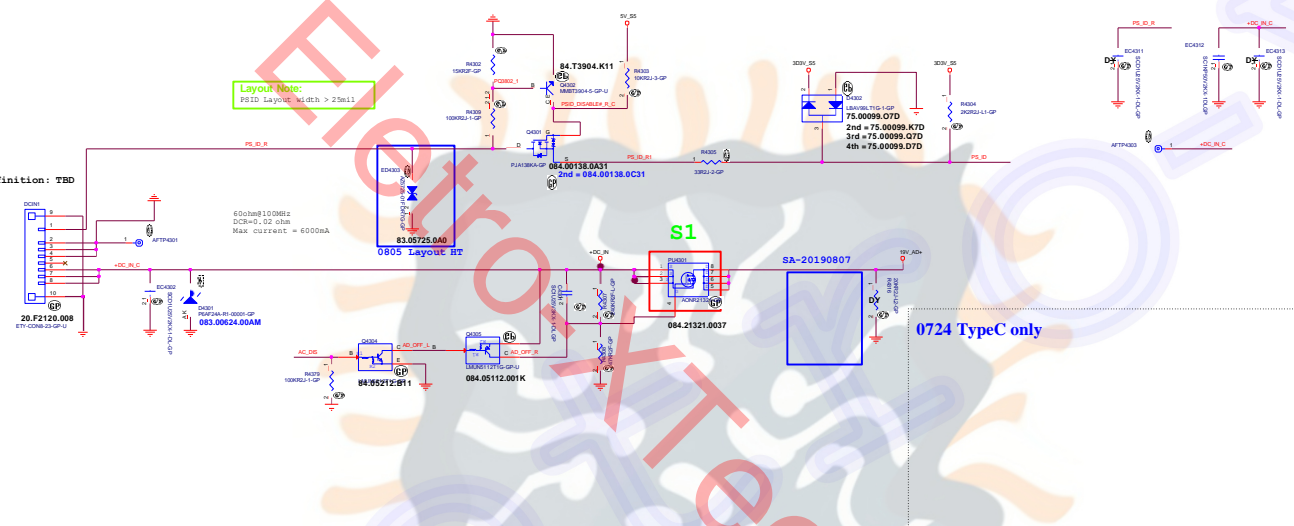
DELL		Wistron Corporation	
		21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, Taippei-Hsien221, Taiwan, R.O.C.	
Title			
USB Charger			
Size	Document Number	Rev	
Custom	Mockingbird CML	SC	
Date:	Monday, December 09, 2019	Sheet 36	of 106



Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

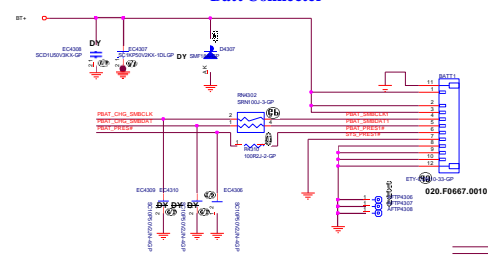


SA-20190807

0724 TypeC only

Main Func = M-BAT Input

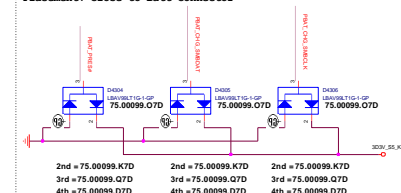
Batt Connector



```

:
:
: Placement: Close to Batt Connector
:
:

```



OFFPAGE

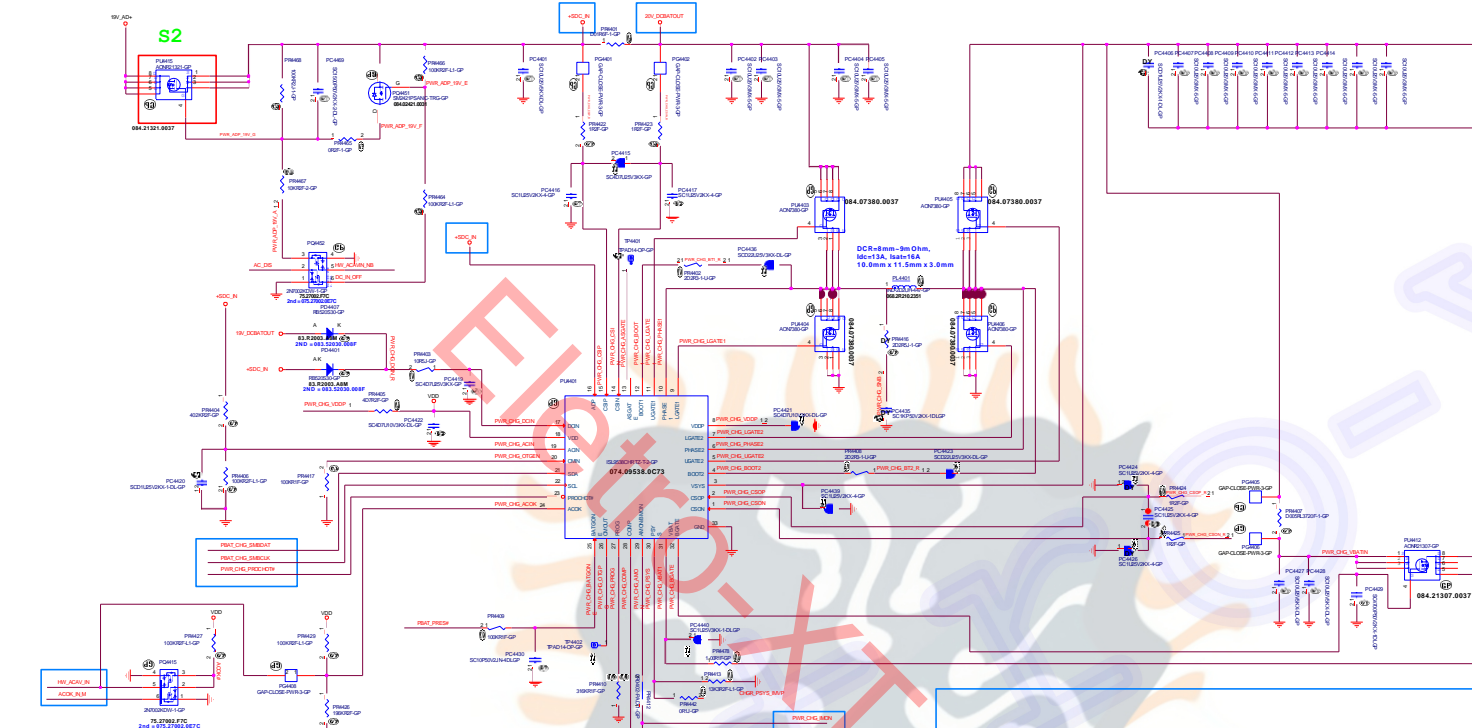


Figure 10: TypeC Prochot. This figure contains three circuit diagrams. The top diagram shows a TypeC Prochot circuit for a GPU side, featuring a PWR_CHL_PROCHOT_R pin connected to a PWRCHL_PROCHOT_R pin, with a 10k resistor and a 10k resistor. The middle diagram shows a TypeC Prochot circuit for a CPU side, featuring a PWRCHL_PROCHOT_R pin connected to a PWRCHL_PROCHOT_R pin, with a 10k resistor and a 10k resistor. The bottom diagram shows a TypeC Prochot circuit for a CPU side, featuring a PWRCHL_PROCHOT_R pin connected to a PWRCHL_PROCHOT_R pin, with a 10k resistor and a 10k resistor.



ISL95859C For CPUCORE

Eleto-XTechnical

PH on CPU side

[33.044] PREDCHY_CPU <<<

[7] SVID_ALERTY_CPU <<<

[7] SVID_CLK_CPU >>>

[7] SVID_DATA_CPU >>>

[17.44] PWR_BMP_PWRGD >>>

[17.24-46.46] VCCST_PWRGD >>>

For VCCGT Sense

[8] VCCGT_SENSE >>>

[8] VCCGT_SENSE >>>

For Vcore Sense

[7] VCCORE_SENSE >>>

[7] VCCORE_SENSE >>>

For Vccsa Sense

[8] VCCSA_SENSE >>>

[8] VCCSA_SENSE >>>

EB side Link

SVID Pull High V



[47] PWR_VCORE_PWMA >>>

[47] PWR_VCORE_ISUM >>>

[47] PWR_VCORE_ISUM >>>

[47] PWR_VCORE_PFCM >>>

[47] PWR_VCORE_PWMA >>>

[47] PWR_VCCGT_PWM >>>

[47] PWR_VCCGT_PFCM >>>

[47] PWR_VCCGT_ISUM >>>

[47] PWR_VCCGT_ISUM >>>

[47] PWR_VCCSA_PWMA >>>

[47] PWR_VCCSA_PWMA >>>

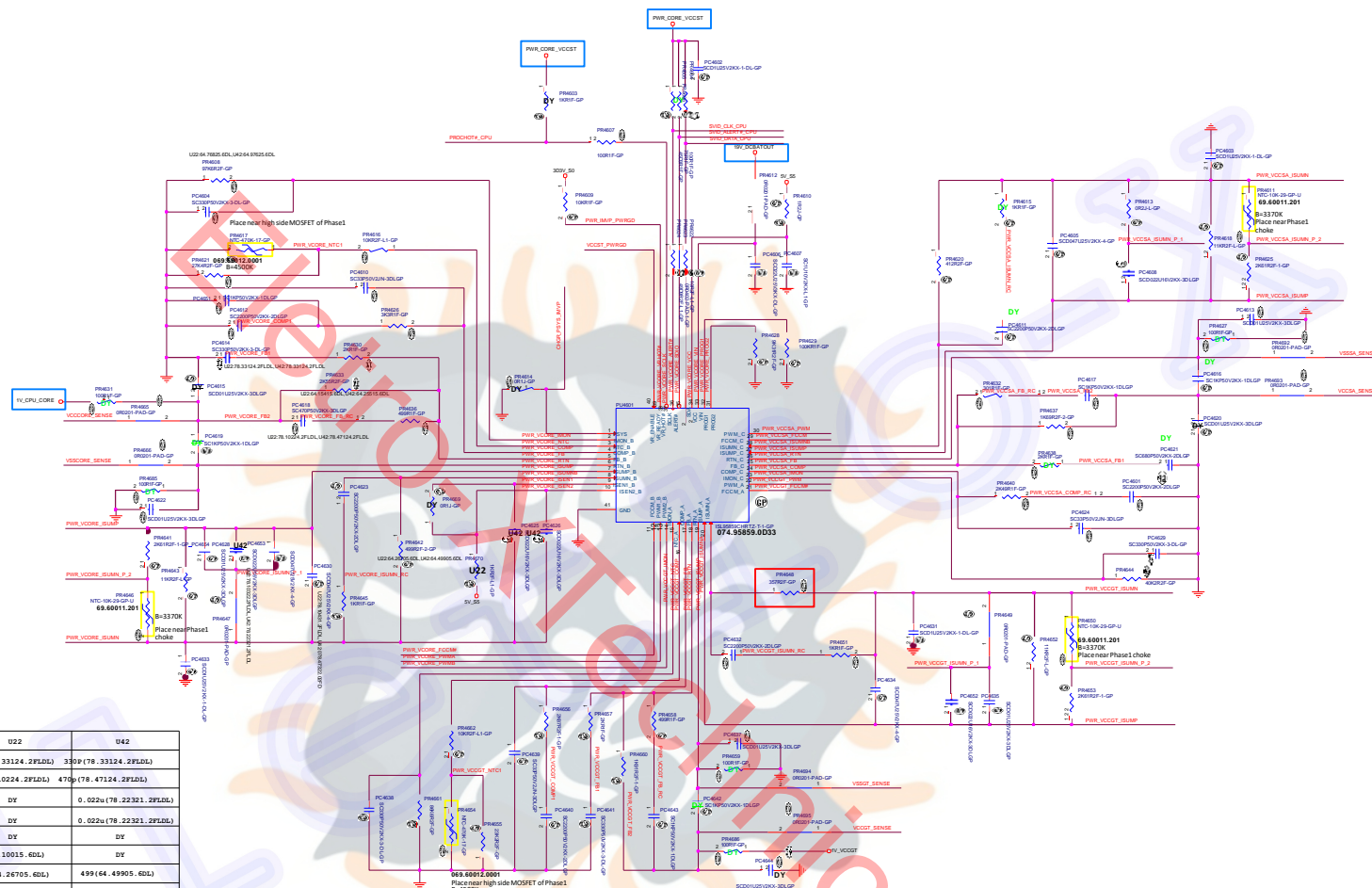
[47] PWR_VCCSA_PFCM >>>

[47] PWR_VCORE_SEN1 >>>

[47] PWR_VCORE_SEN2 >>>

[46] CHRG_PSTY_BMP >>>

	U22	U42
PC4614	30pF(78.33124.2PFLDL)	30pF(78.33124.2PFLDL)
PC4615	30pF(78.10224.2PFLDL)	470pF(78.47124.2PFLDL)
PC4625	DY	0.022uF(78.22321.2PFLDL)
PC4626	DY	0.022uF(78.22321.2PFLDL)
P84669	DY	DY
P84670	1K(64.10015.6DL)	DY
P84642	267(64.26705.6DL)	499(64.49905.6DL)
PC4630	0.1uF(78.10431.2PFLDL)	47uF(78.47322.02PDL)
PC4628	0.01uF(78.10322.2PFLDL)	20uF(78.22321.2PFLDL)
PC4654	DY	0.01uF(78.10322.2PFLDL)
PC4653	DY	47uF(78.47322.02PDL)
P84633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
P84608	7.8K(64.76825.6DL)	97.6K(64.97625.6DL)

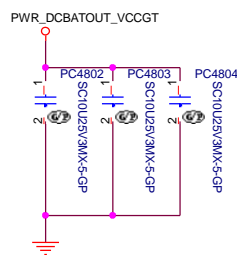
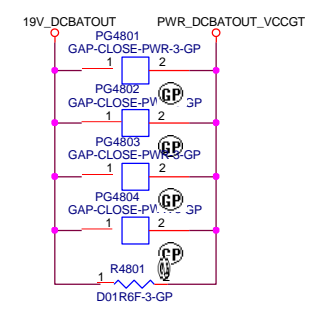


Eleto-XTechnical

Eleto-XTechnical

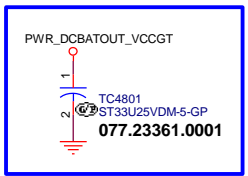
Main Func = CPU_CORE

Offpage-Signal



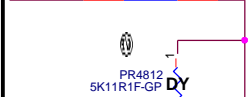
AOZ5516Q For VCCGT

For acoustic noise



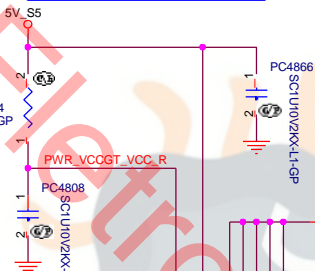
[46] PWR_VCCGT_PWM
[46] PWR_VCCGT_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN

PR4802
0R0201-PAD-GP



PWR_VCCGT_FCCM#

PWR_VCCGT_FCCM#



PWR_VCCGT_VCC_R

PWR_VCCGT_BOOT_RC

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

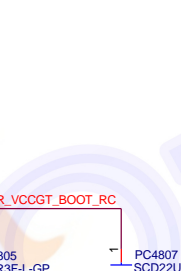
PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

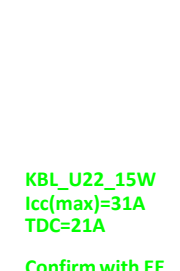
PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

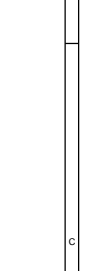
PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT



PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

PWR_VCCGT_BOOT

KBL_U22_15W
Icc(max)=31A
TDC=21A

Confirm with EE
22uF/0805 total 33pcs
(78.22610.L2L)

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Isc : 37A , Isat : 41A

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT


1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT

1V_VCCGT




Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin,
Taipei-Hsien 221, Taiwan, R.O.C.

Title: **POWER (5516_CPU_VCORE(13))**

Size: A3

Date: Monday, December 09, 2019

Sheet: 48 of 48



Mockingbird CML

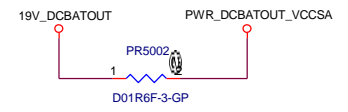
Eleto-XTechnical

Eleto-X

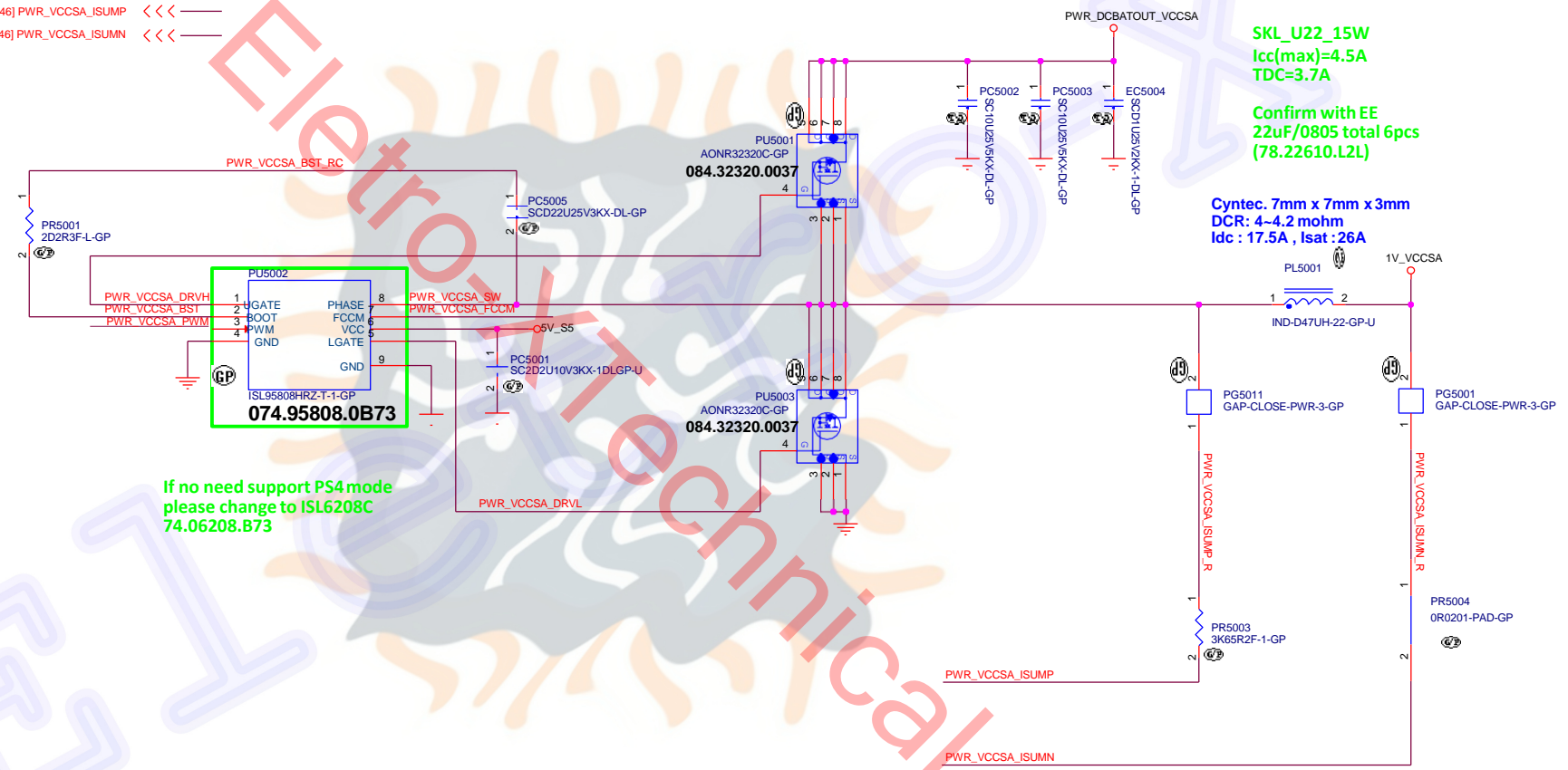
ISL95808 For VCCSA

Eleto-XTechnical

OFFPAGE



[46] PWR_VCCSA_PWM >>>
[46] PWR_VCCSA_FCCM >>>
[46] PWR_VCCSA_ISUMP <<<
[46] PWR_VCCSA_ISUMN <<<




SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A


Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

Cytec. 7mm x 7mm x 3mm
DCR: 4~4.2 mohm
Icc: 17.5A, Isat: 26A

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

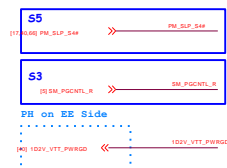
**Wistron Corporation**
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
Taipei-Hsien 221, Taiwan, R.O.C.

Title	POWER (ISL95808_VCCSA)		
Size	A3	Document Number	Mockingbird CML
Date	Monday, December 09, 2019	Sheet 50	of 50

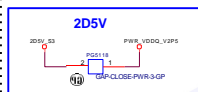
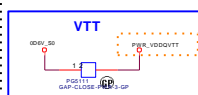
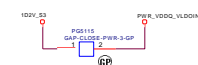
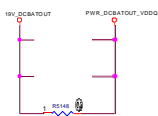


Eleto-XTechnical

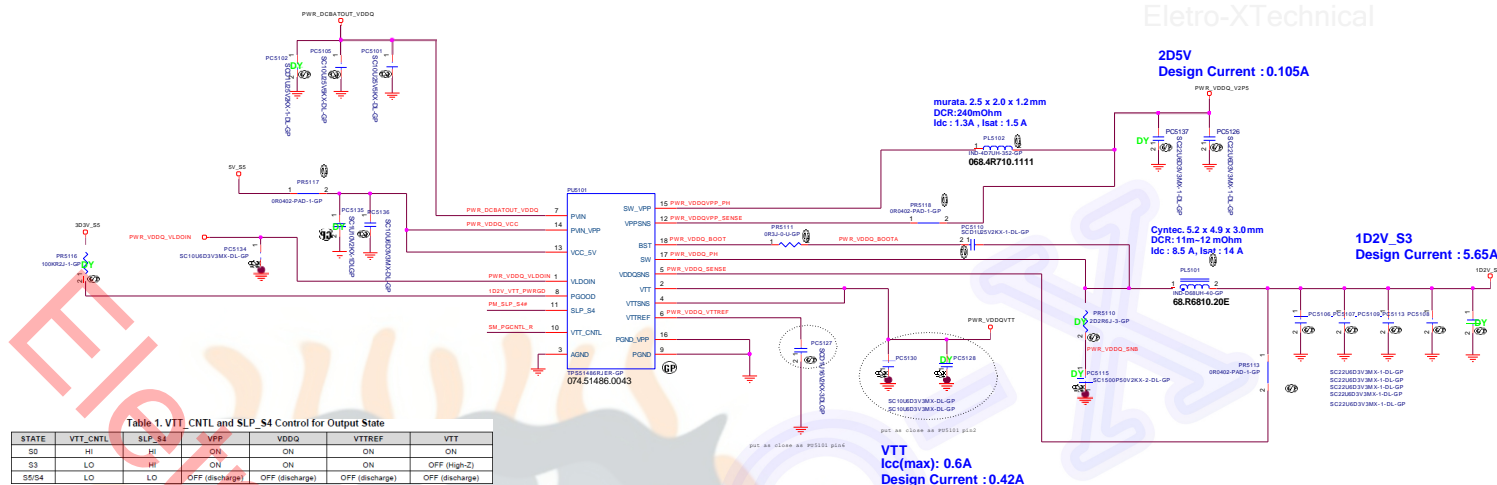
OFFPAGE



OFFPAGE GAP



STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
SKIR	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)



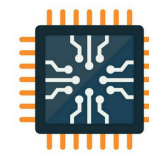
2D5V
Design Current : 0.105A

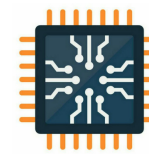
Cyntec. 5.2 x 4.9 x 3.0 mm
DCR: 11m~12 mOhm
Idc : 8.5 A, Isat : 14 A

1D2V_S3
Design Current : 5.65A

VTT
I_{cc}(max): 0.6A
Design Current : 0.42A

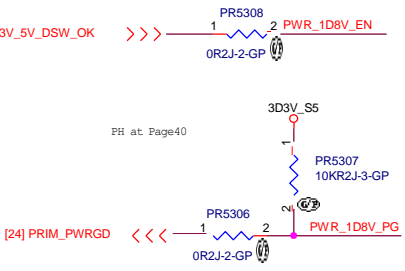
<Corne Design



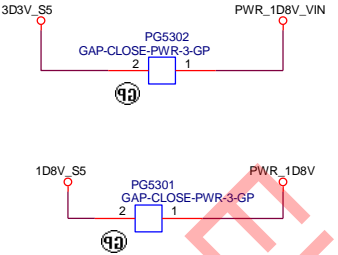


Main Func = 1D8V

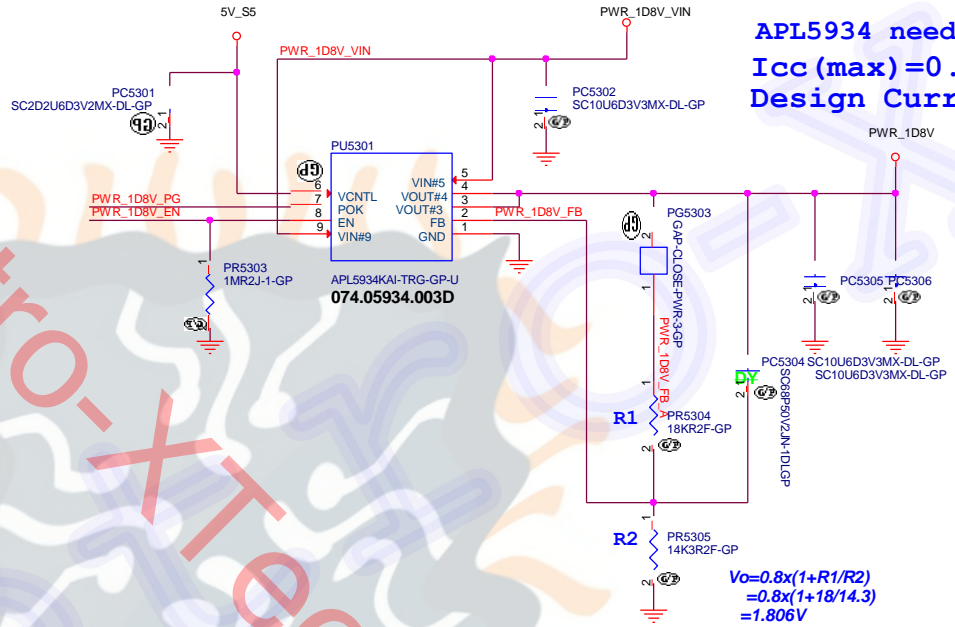
OFFPAGE



OFFPAGE_GAP



APL5934 for 1D8V



APL5934 need <1.8W
Icc (max) = 0.95A
Design Current = 0.82A

$$V_o = 0.8 \times (1 + R1/R2)$$
$$= 0.8 \times (1 + 18/14.3)$$
$$= 1.806V$$

Eletr-XTechnical

Eletr-XTechnical

Eletr-X

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin,
Taipei-Hsien 221, Taiwan, R.O.C.

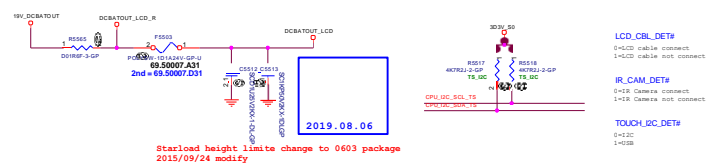
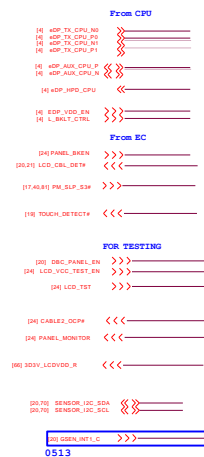
Title: **POWER (APL5934 1D8V)**

Size: A3 Document Number: **Mockingbird CML**

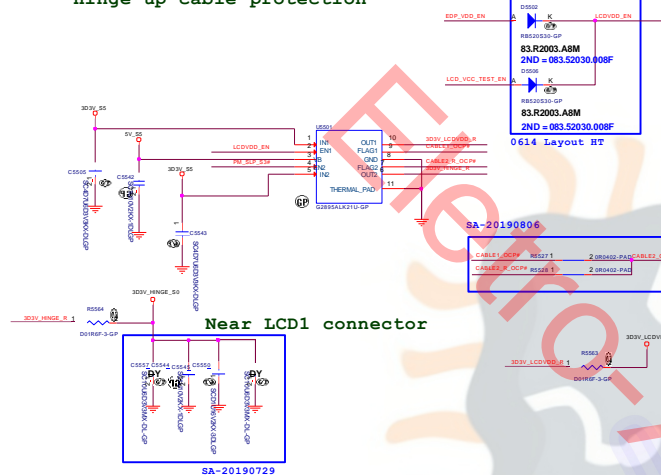
Date: Monday, December 09, 2019 Sheet 59 of 1

Main Func = LCD

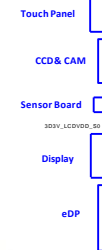
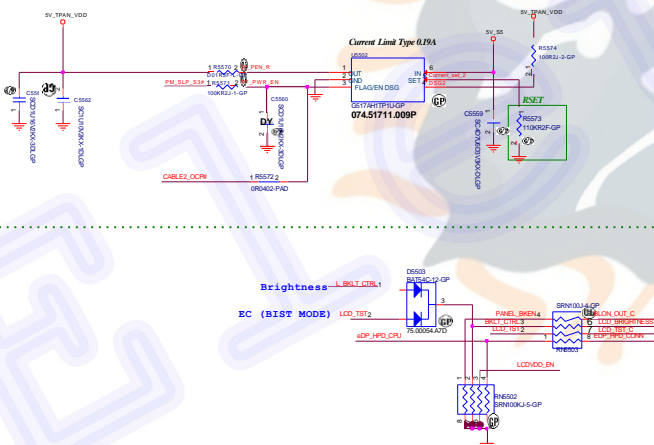
INVERTER POWER



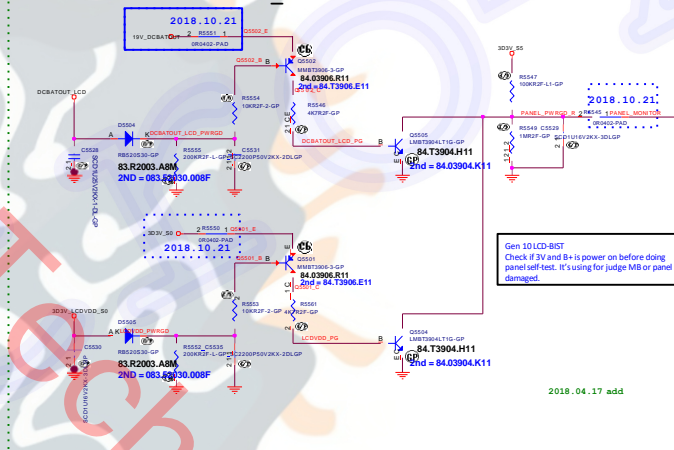
Hinge up cable protection



Current Limit Type 0.19A



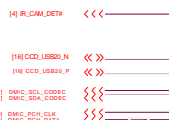
PANEL_PWRGD CIRCUIT



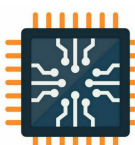
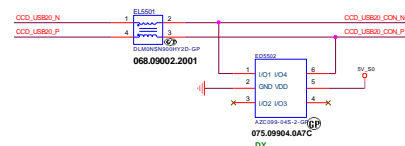
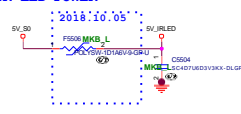
Main Func = Touch panel



Main Func = CAMERA



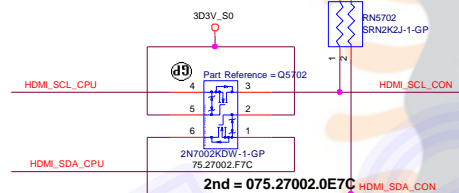
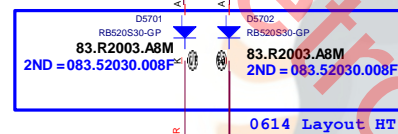
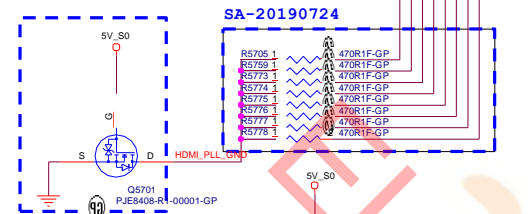
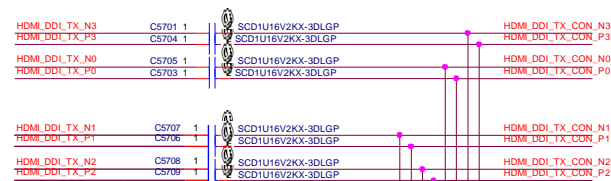
IR LED POWER



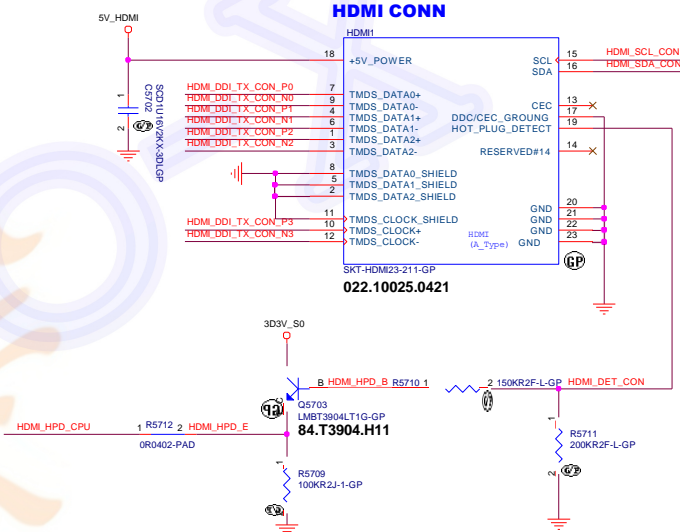
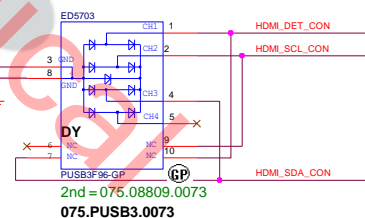
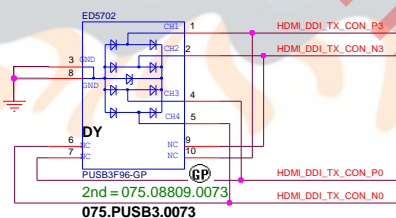
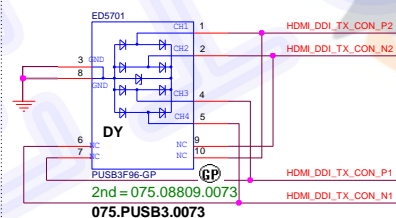
SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N3
[4] HDMI_DDI_TX_P3

[4] HDMI_SCL_CPU
[4] HDMI_SDA_CPU
[4] HDMI_HPD_CPU

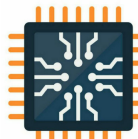


EMI Request:



<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title		HDMI	
Size	Document Number	Rev	SC
Custom	Mockingbird CML		
Date:	Monday, December 09, 2019	Sheet 57	of 106

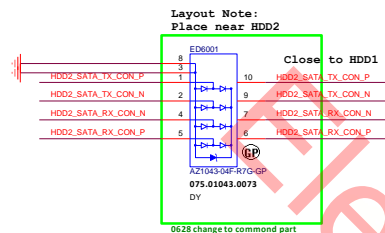


[70] FFS_INT2_Q >>> _____
[16.60] HDD_DEVSLP >>> _____

[16] HDD_SATA_TX_P >>> _____
[16] HDD_SATA_TX_N >>> _____
[16] HDD_SATA_RX_P <<< _____
[16] HDD_SATA_RX_N <<< _____
[16.60] HDD_DEVSLP <<< _____
[16] HDD_DET# <<< _____

HDD POWER

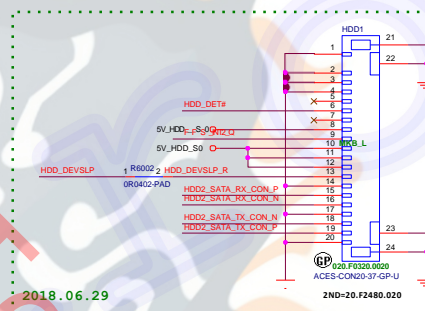
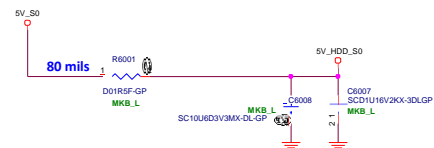
Eletro-XTechnical



SATA HDD Connector

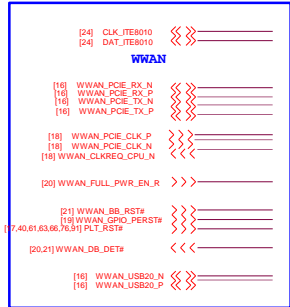
COLAY WITH: R1611/R1612/R1607/R1608

HDD_SATA_TX_P C6028 1 SC0D01U25V20X-30LGP HDD2_SATA_TX_CON_P
HDD_SATA_TX_N C6029 1 SC0D01U25V20X-30LGP HDD2_SATA_TX_CON_N
HDD_SATA_RX_N C6030 1 MKB L SC0D01U25V20X-30LGP HDD2_SATA_RX_CON_N
HDD_SATA_RX_P C6031 1 MKB L SC0D01U25V20X-30LGP HDD2_SATA_RX_CON_P

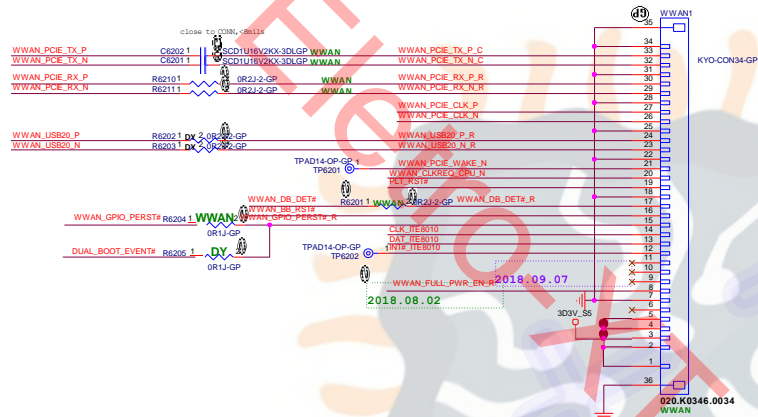


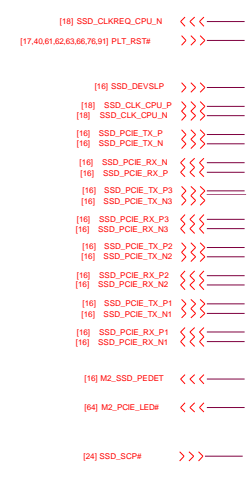
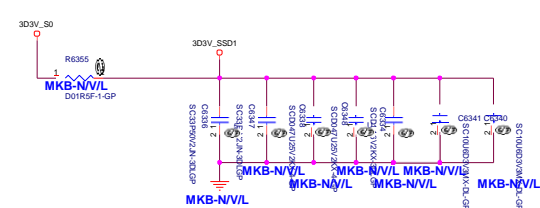
Eletro-XTechnical

Eletro-X

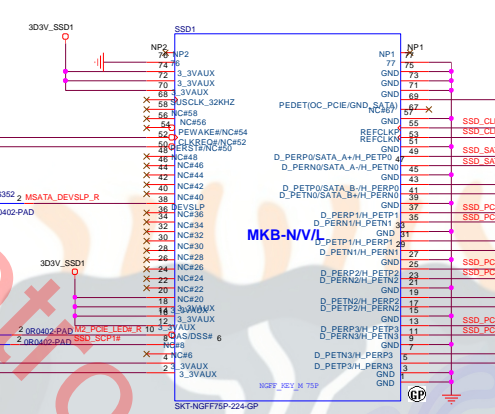


[16] DUAL_BOOT_EVENTS# >>> _____





SSD M.2 CONN



PCIE:1 SATA:0

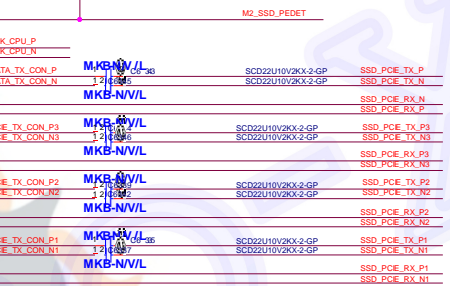


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

[illegible]

Table 13-12.SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 2 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 2/ SR
Processor I/s	100 nf	220 nf	10 nf	100 nf	220 nf
Processor R/s	None	None	10 nf	None	None

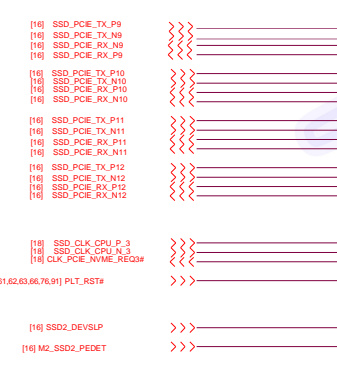
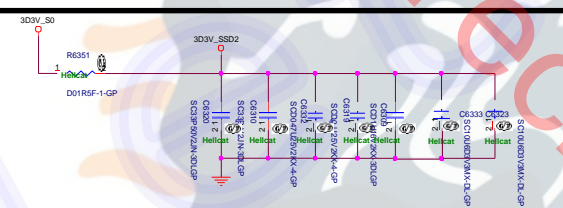
Design-Constraint: For PCA only application, please refer to the PCA guidelines for design.
Design-Constraint: For PCA only application, both TX and RX channels need to have 10-fF capacitors on the motherboard. This option supports all SATA devices. However, the RX 10 of capacitor can support 15.5 Gbps SATA Gen 3 SATA multilayer configurations, motherboard TX requires an 18G AC capacitor and RX AC capacitor is required for motherboard TX channel. **This option DOES NOT support DC coupled D0/D16 devices.**

Design-Constraint: For PCA* Gen 3 SATA multilayer configurations, motherboard TX requires a 22G AC capacitor and RX AC capacitor is required for motherboard TX channel. **This option DOES NOT support DC coupled D0/D16 devices.**

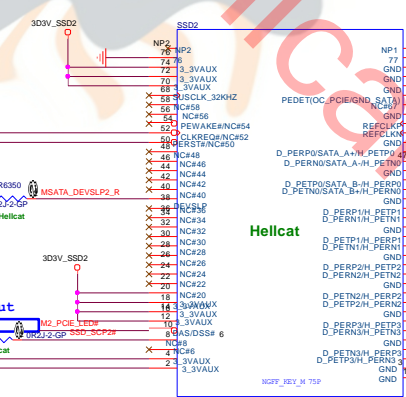
Design-Constraint: As required to the Chapter 3, "General Differential Signal Design Guidelines" along with the additional guidelines in this section for all design optimization purposes.

Design-Constraint: For PCA* Gen 3 SATA multilayer configurations, motherboard TX requires a 22G AC capacitor and RX AC capacitor is required for motherboard TX channel. **This option DOES NOT support DC coupled D0/D16 devices.**

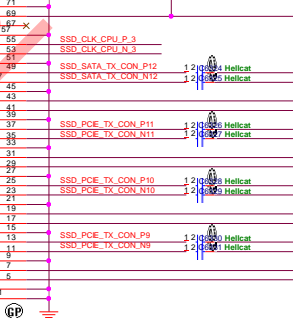
M.2 SSD2



SSD M.2 CONN



PCIE:1 SATA:0



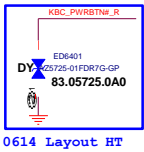
0618 For Layout



SKT-NGFF75P-224-GP
062.10003.0F31
2nd =062.10003.048
3rd =062.10003.0F21

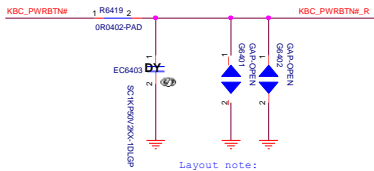
Main Func = Power BTN

[20,24,66] LID_CL_SIO# <<< _____
[24] KBC_PWRBTN# <<< _____
[66] KBC_PWRBTN#_R <<< _____



0614 Layout HT

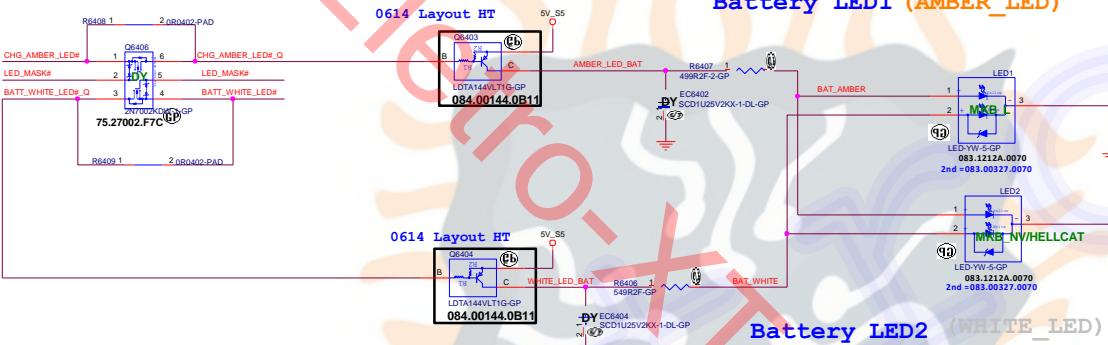
Power button



Layout note:
G6401 place to bottom
G6402 place to top

Main Func = Battery LED

Low activated from KBC GPIO
[24,66] LED_MASK# >>> _____
[24] CHG_AMBER_LED# >>> _____
[24] BATT_WHITE_LED# >>> _____



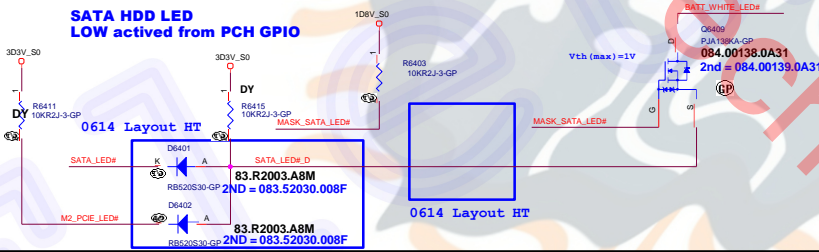
0614 Layout HT

Battery LED1 (AMBER_LED)

Battery LED2 (WHITE_LED)

Main Func = HDD LED

[24] MASK_SATA_LED# >>> _____
[16] SATA_LED# >>> _____
[63] M2_Pcie_LED# <<< _____

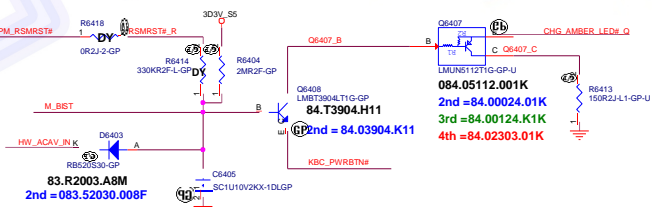


SATA HDD LED
LOW activated from PCH GPIO

0614 Layout HT

Main Func = M-BIST

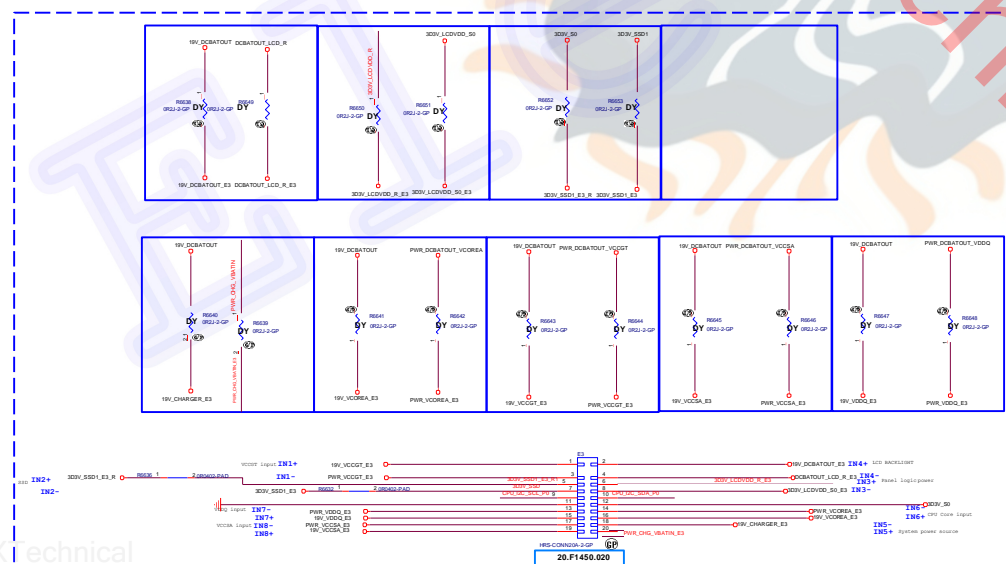
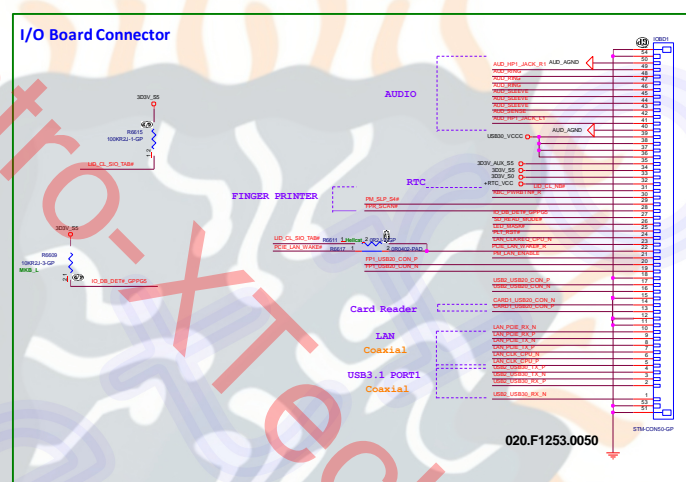
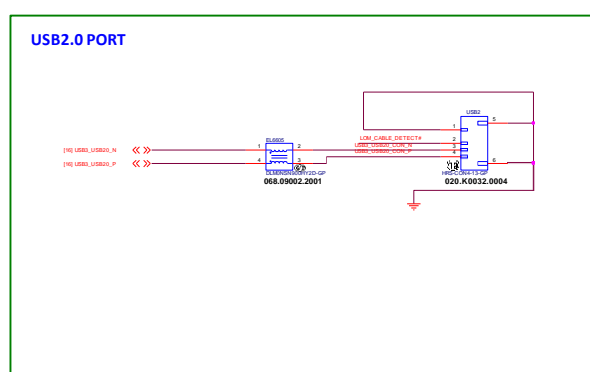
[17] PM_RSMRST# >>> _____
[24] M_BIST >>> _____
[24,44] HW_Acay_IN >>> _____



Wistron Corporation
2/F, No. 101, Hsinchu Rd., Hsinchu,
Taiwan 30001, Taiwan, R.O.C.

LED Board&Power Button

Size	Document Number	Rev
Custom	Mockingbird CML	SC
File	File	File



ESPI

[18,24] ESPI_CLK >>> _____

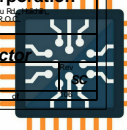
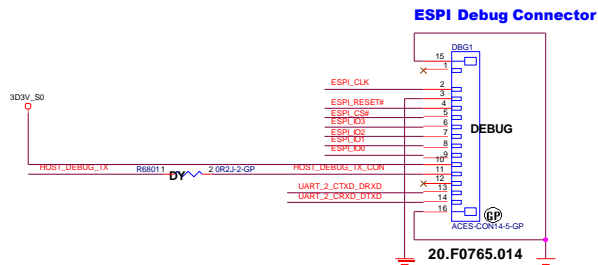
[18,24] ESPI_RESET# >>> _____

[18,24] ESPI_CS# >>> _____

[18,24] ESP_IDO[3..0] << >> ESP_ID3
ESP_ID2
ESP_ID1
ESP_ID0

UART

```
[24] HOST_DEBUG_TX      >>>_____
[20] UART_2_CTXD_DRXD    >>>_____
[20] UART_2_CRXD_DTXD    <<<_____
```



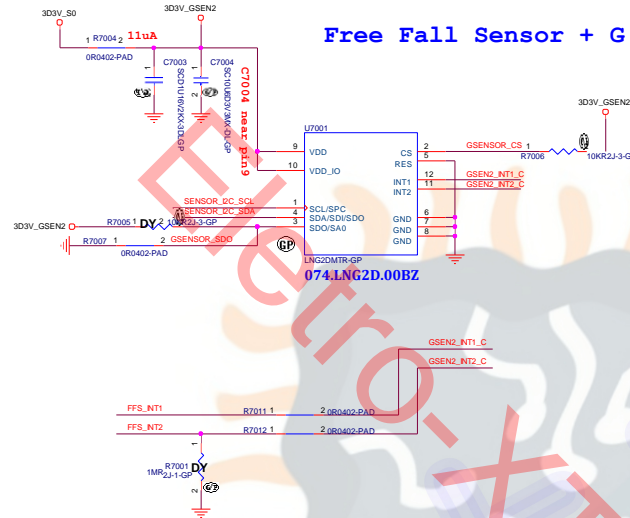
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

Eletro-XTechnical

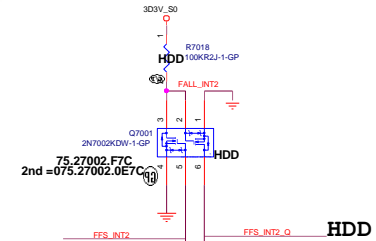
The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

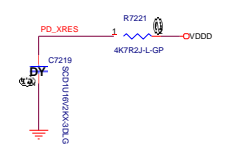
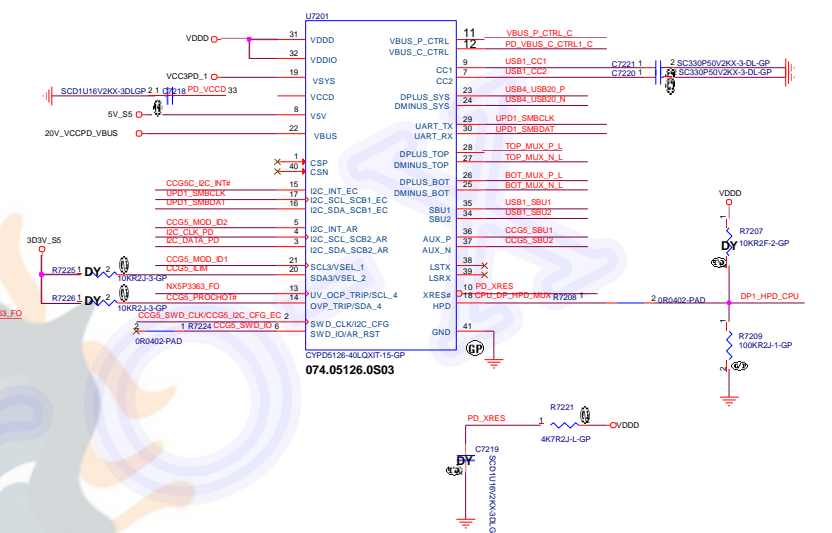
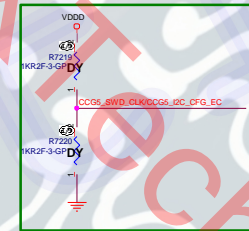


Note:

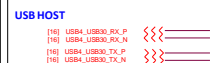
- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

Eletro-XTechnical

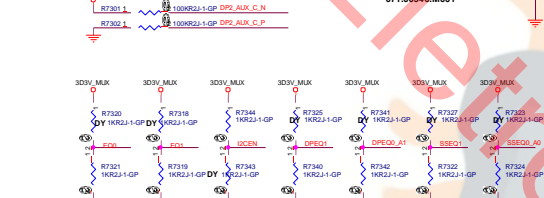
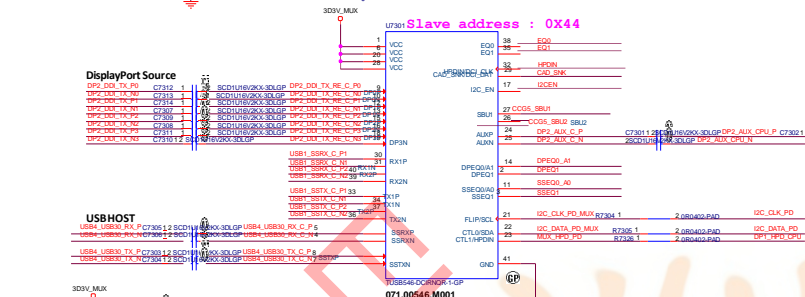
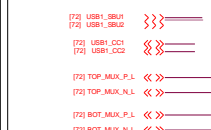
Eletro-X



- DisplayPort Source

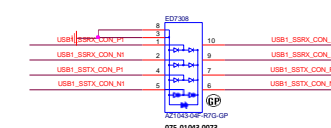
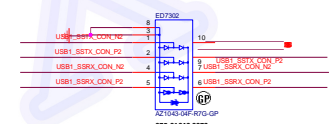
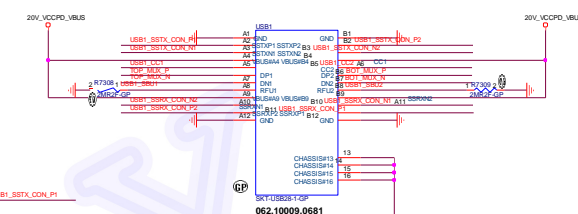
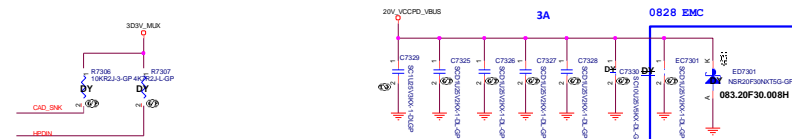


TypeC CC

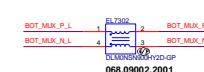
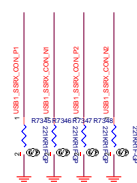
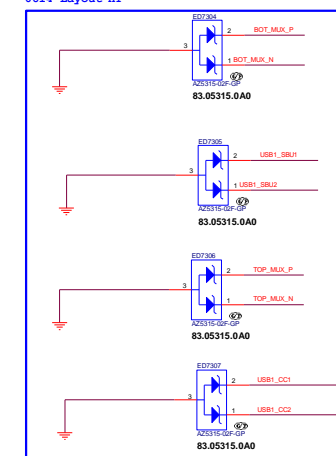


Host	Kernel	GPU	Host Operation
H	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation
HIGH	HIGH	LOW	USB3.1 only orientation

	DCI	nonDCI
23 CCLK/HFOUT	DP Enable in GPIO mode RFD in I2C mode	DP Enable in GPIO mode Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Group EN in GPIO mode DCI DAT in I2C mode	AUX Group EN in GPIO mode EN in I2C mode
32 DCI_CLK	RFD in GPIO mode	RFD

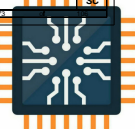


0614 Layout HT



-Como Descobri

Eletro-XTechnica





[18] GFX_CLK_CPU_P >>>
 [18] GFX_CLK_CPU_N >>>
 [20] DOPU_HOLD_RSTN >>>
 [17] ALB16060601PLT_RSTN >>>
 [16] VGACORE_VDD_SENSE_1 <<<
 [16] VGACORE_GND_SENSE_1 <<<

[16] CLK_POE_PEG_REG# <<<
 [16] GFX_POE_RX_P0 <<<
 [16] GFX_POE_RX_N0 <<<
 [16] GFX_POE_TX_P0 <<<
 [16] GFX_POE_TX_N0 <<<
 [16] GFX_POE_RX_P1 <<<
 [16] GFX_POE_RX_N1 <<<
 [16] GFX_POE_TX_P1 <<<
 [16] GFX_POE_TX_N1 <<<

0508

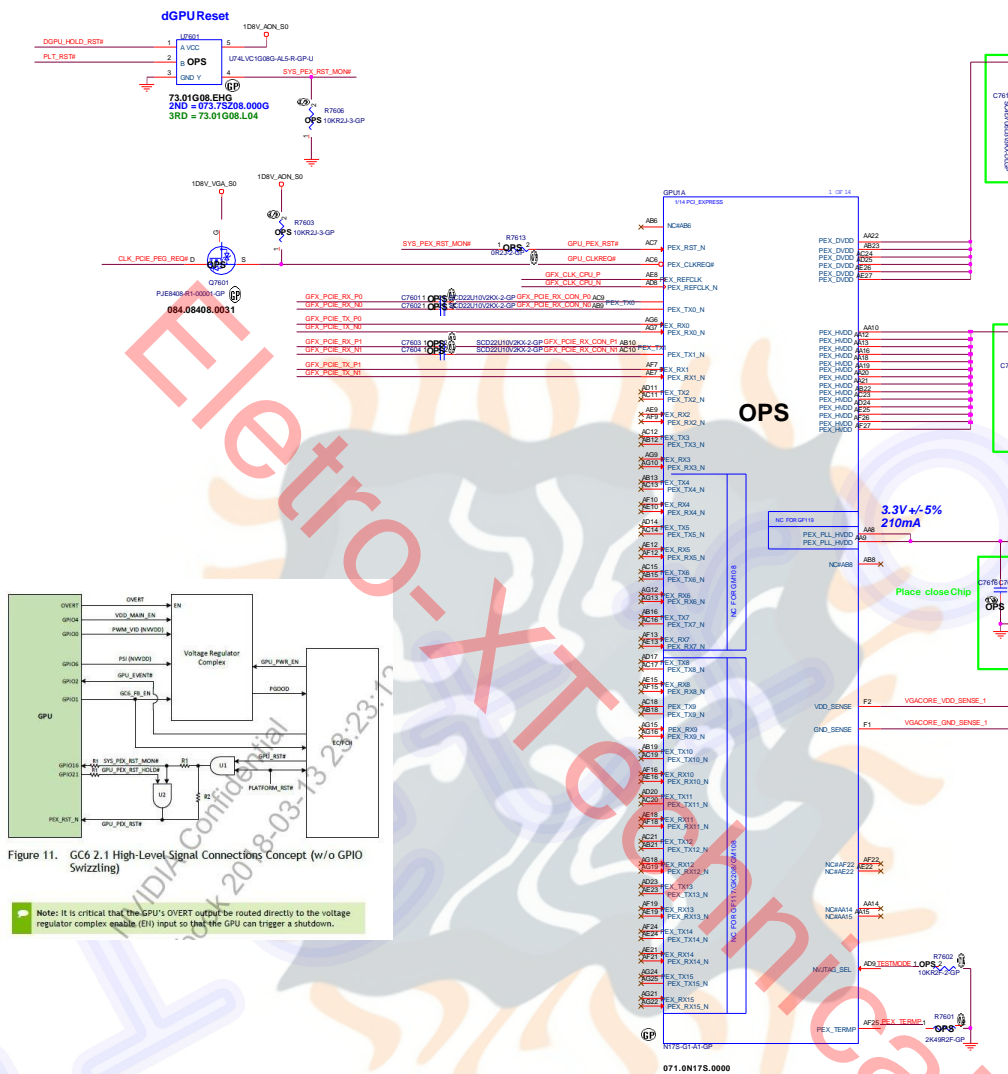


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (E1) input so that the GPU can trigger a shutdown.

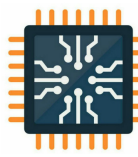
Table 6. PEX Core and IO Supply Decoupling and Filtering

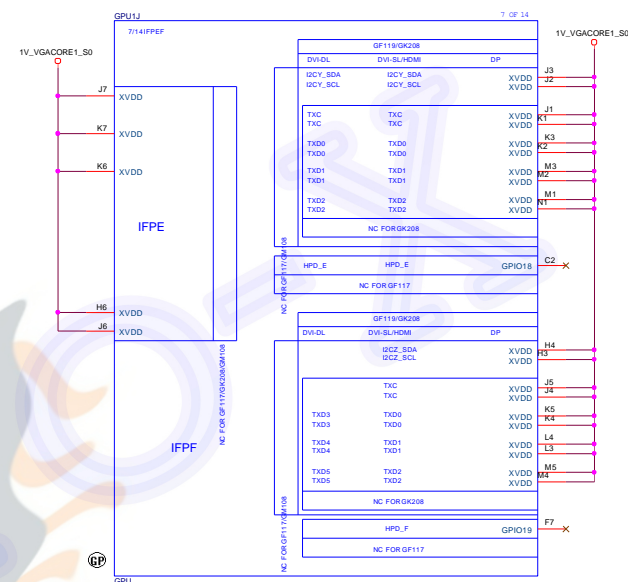
GPU	Capacitor Type	Footprint	Population	N16	N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB28-44, GB2C-44	1.0 μ F X65	0402	1	1		Under GPU
	4.7 μ F X65	0603	0	1		Under GPU
	4.7 μ F X65	0603	2			Near GPU
	10 μ F X65	0805	0	2		Midway between GPU and Power Supply
	22 μ F X65	0805	0	1		Midway between GPU and Power Supply
N16 PEX_IOVDD (N17 PEX_HVDD) Supply Rail						
GB28-44, GB2C-44	1.0 μ F X65	0402	1	4		Under GPU
	4.7 μ F X65	0603	1	2		Near GPU
	10 μ F X65	0805LP	1	2		Midway between GPU and Power Supply
	22 μ F X65	0805LP	1	1		Midway between GPU and Power Supply

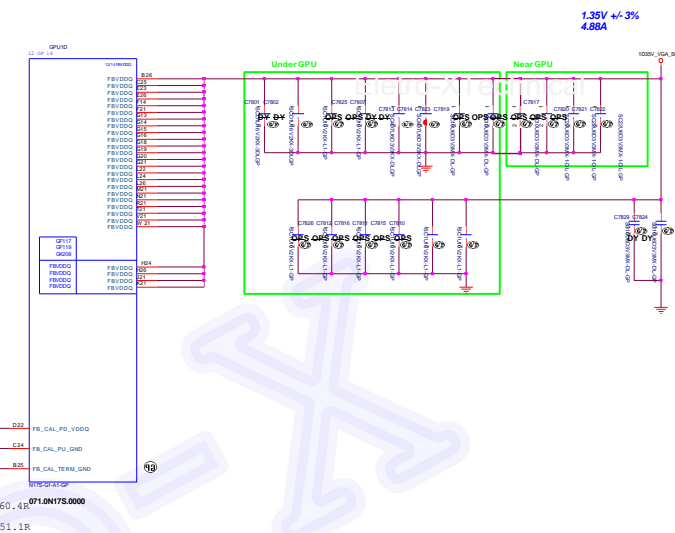
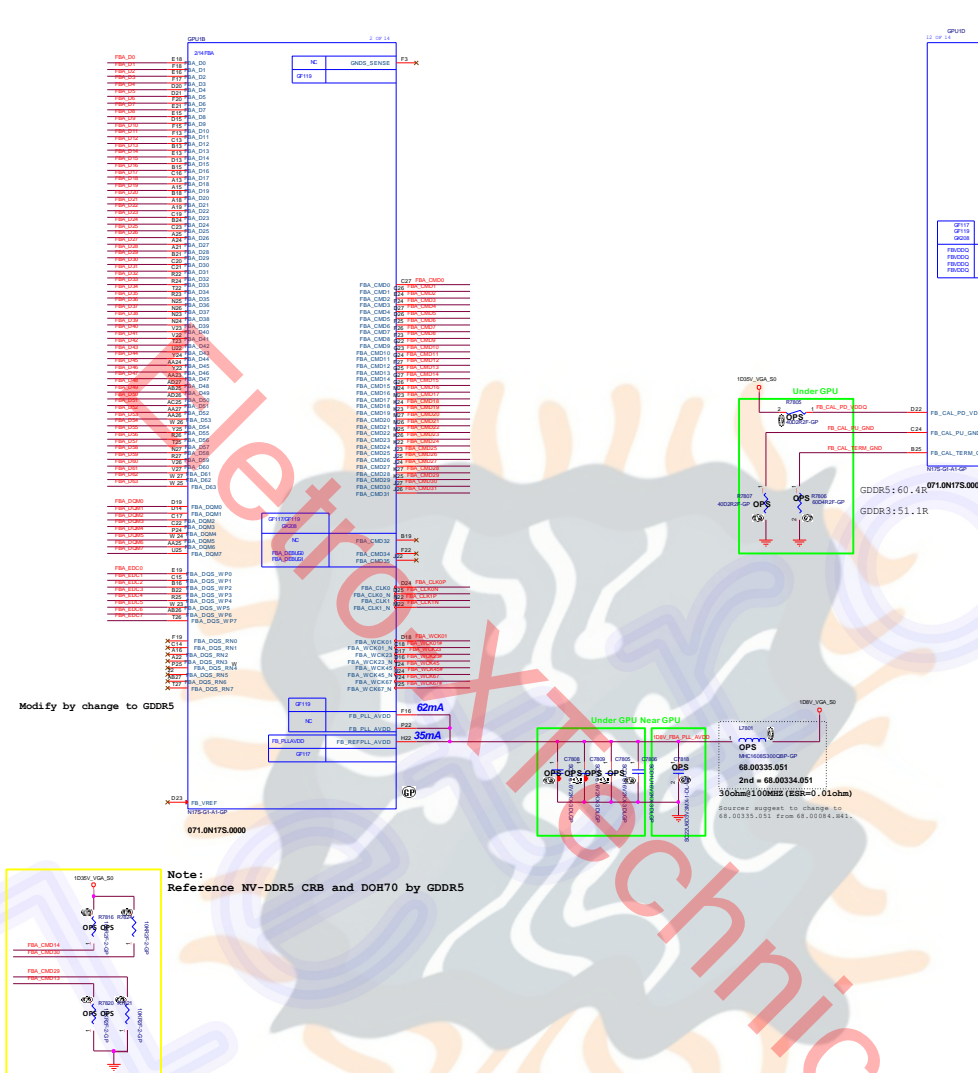
GPU	Capacitor Type	Footprint	Population	N16	N17	Location
PEX_PL1_HVDD Supply Rail						
GB28-44, GB2C-44	0.1 μ F X7R	0402	1	1		Near GPU

Core Design

Wistron Corporation
 21F, 8th, Sec. 1, Hsin-Tsuen Rd., Hsinchu, Taiwan, R.O.C.
GPU(15)/PEG
 Mockingbird CML
 SC

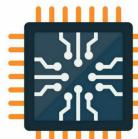






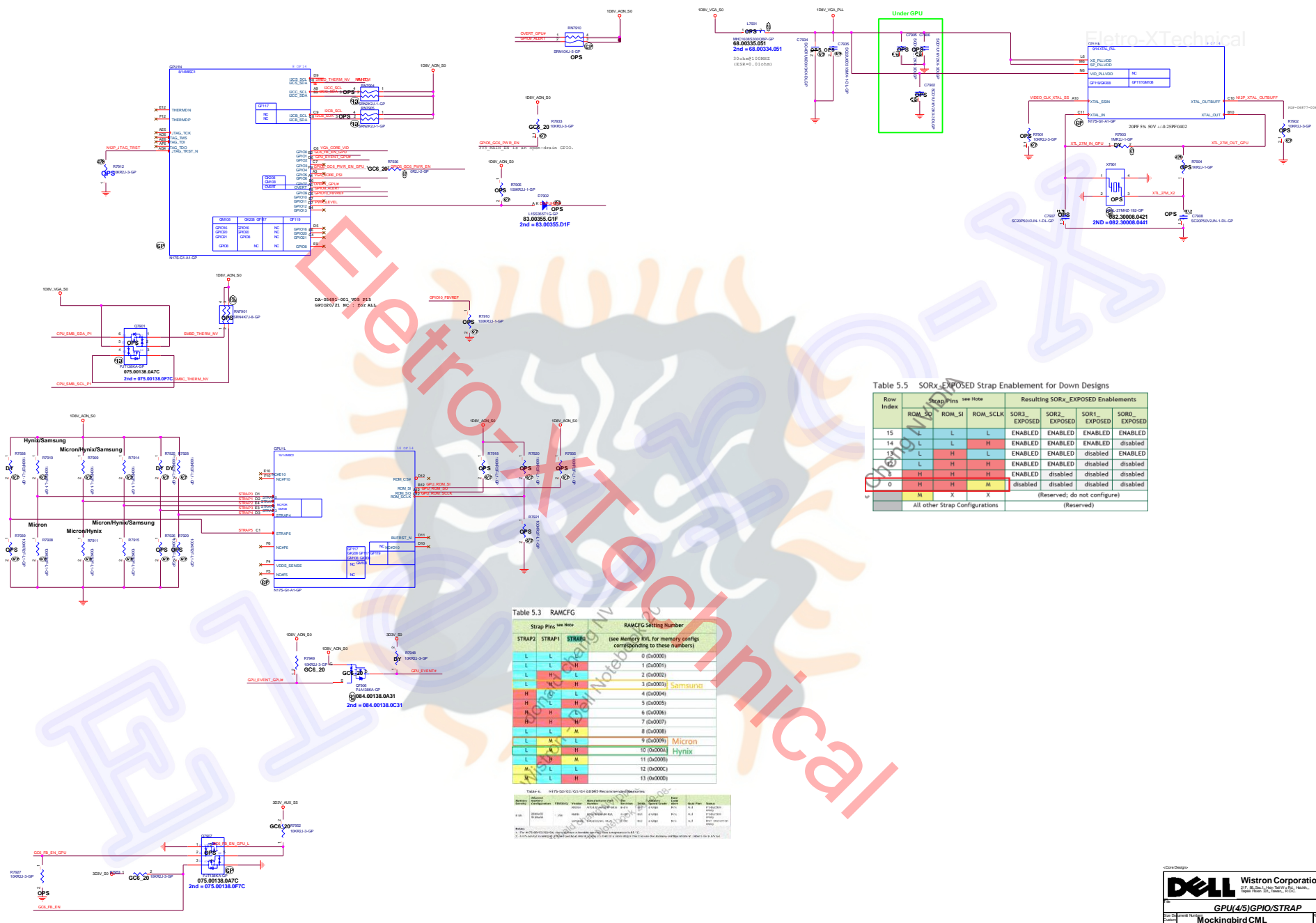
GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
FBVDD/G Supply Rail for GDDR5					
G82B-64, G82C-64	0.1 μ F	X7R 0402	2	0	Under GPU
	1 μ F	X7R 0603	2	8	Under GPU
	4.7 μ F	X6S 0603	2	0	Under GPU
	10 μ F	X6S 0603	0	2	Under GPU
	10 μ F	X6S 0603	1	1	Near GPU
	22 μ F	X6S 0603W	1	3	Near GPU

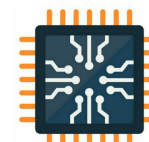
GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 μ F	X7R	0402	2	4	Under GPU
	22 μ F	X6S	0805	1	1	Near GPU
Bead Type						
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

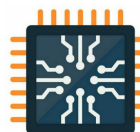
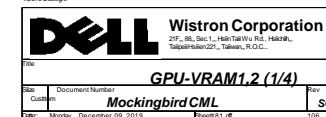


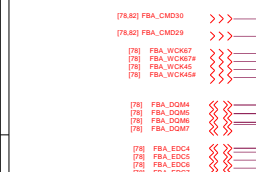
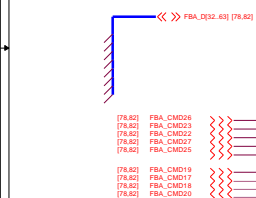
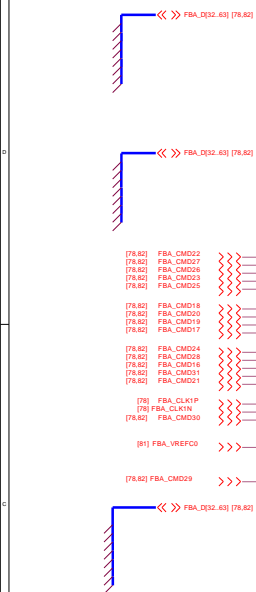
Main Func = dGPU

```
[20] GPU_EVENT# >>>
[85,86] GPIO_CG6_PWR_EN <<<
[24,44] DGPUID# >>
[81] GPIO_FBREF <<<
[85] VGA_CORE_PSI <<<
[85] VGA_CORE_VSD <<>
[20,86] GCE_FLEN <<<
[18,24,26] CPU_SMB_SDA_P1 <<>
[18,24,26] CPU_SMB_SCL_P1 <<>
```



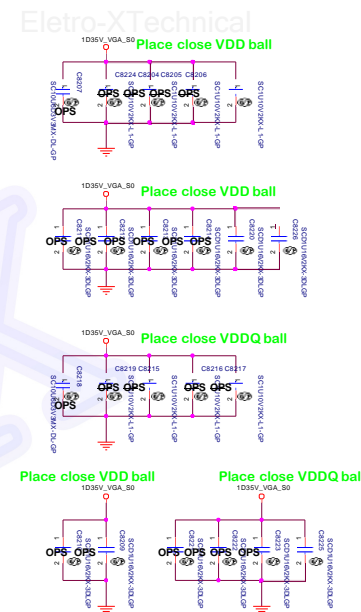
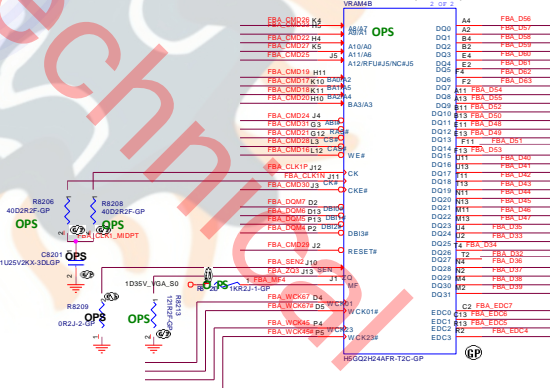
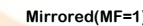
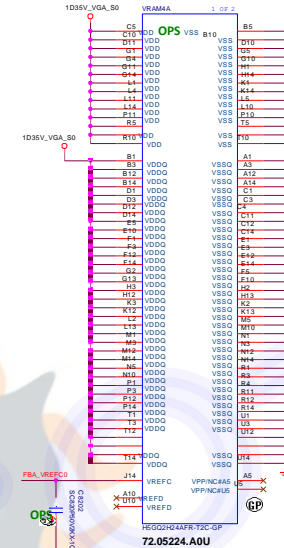




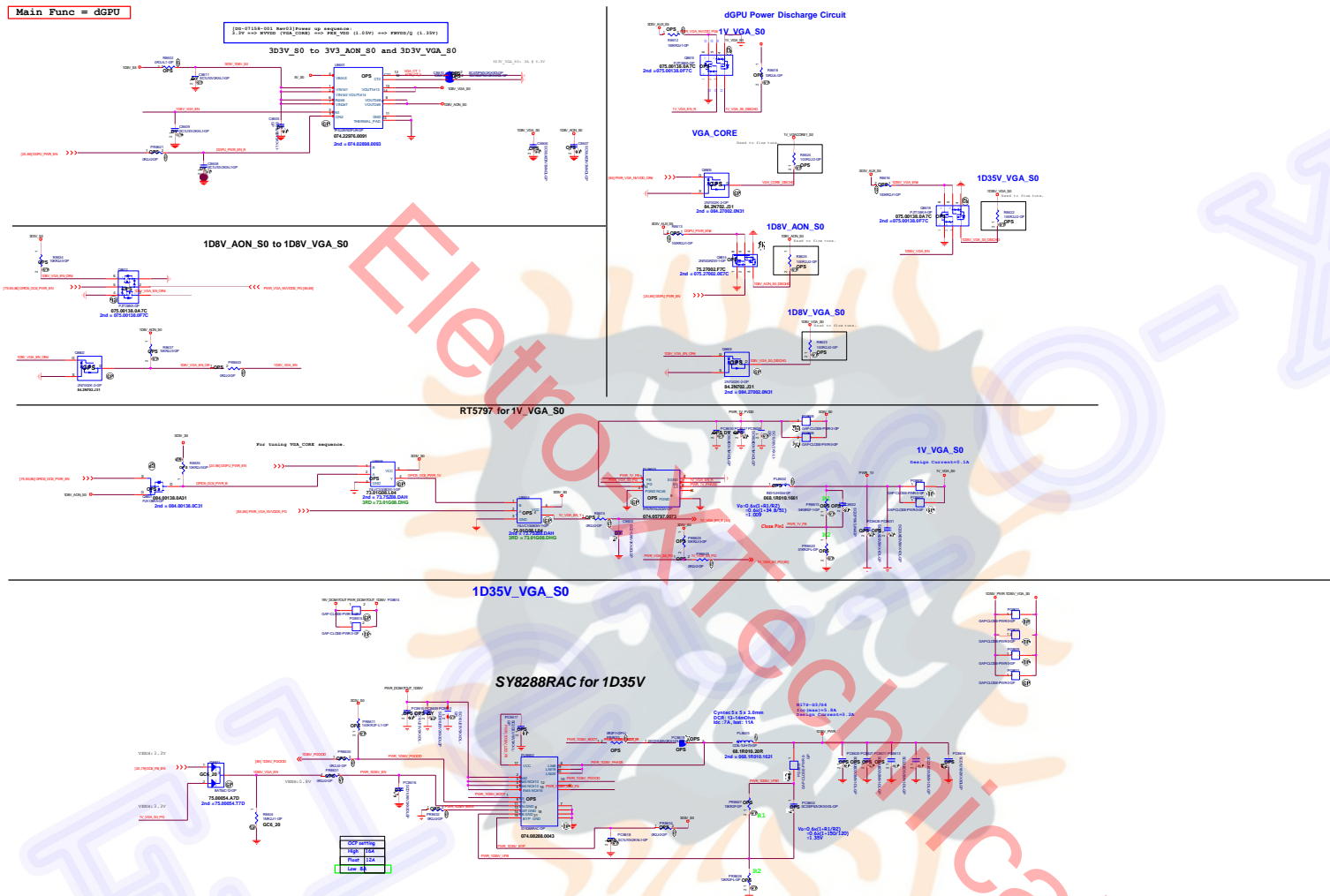


Frame Buffer Partition A-Upper Half

Type	FBVREF%	Voltage	GPU_GPIO1
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



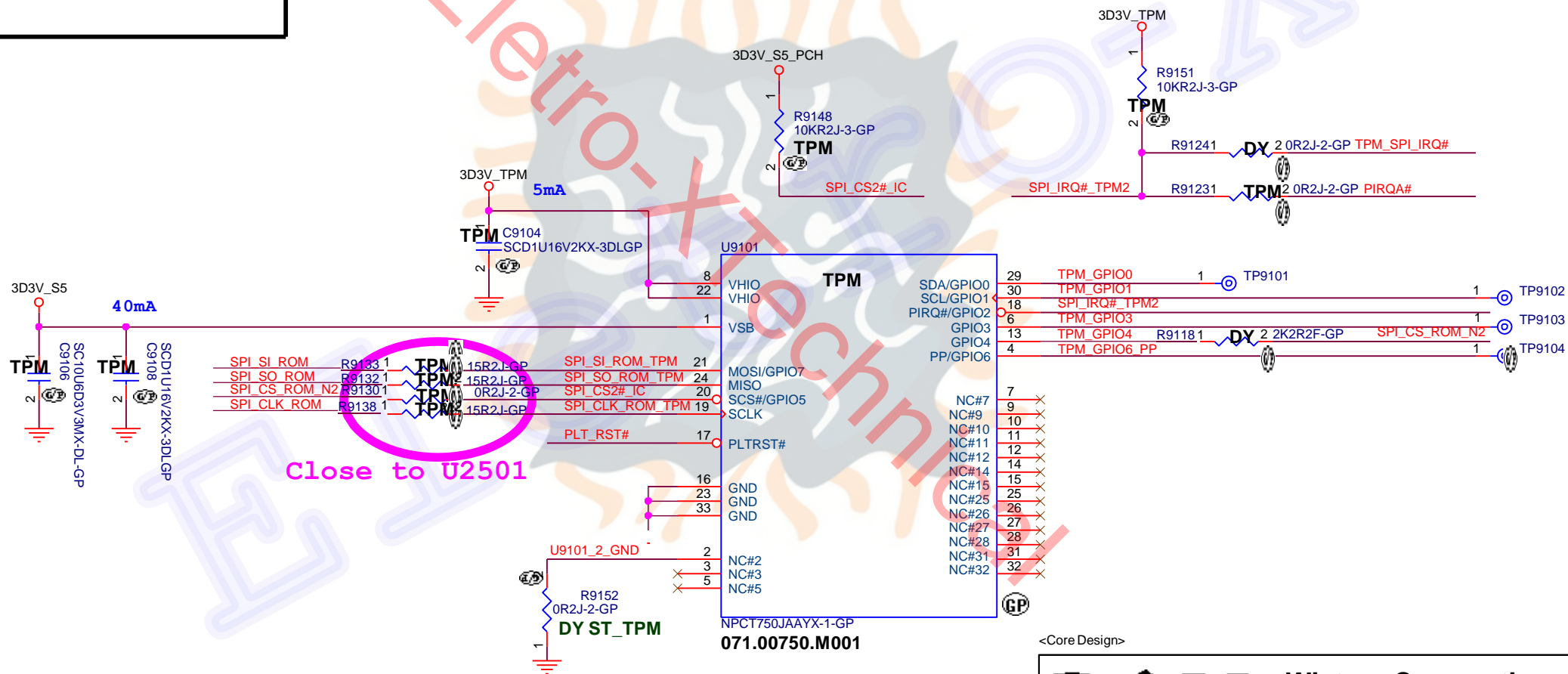
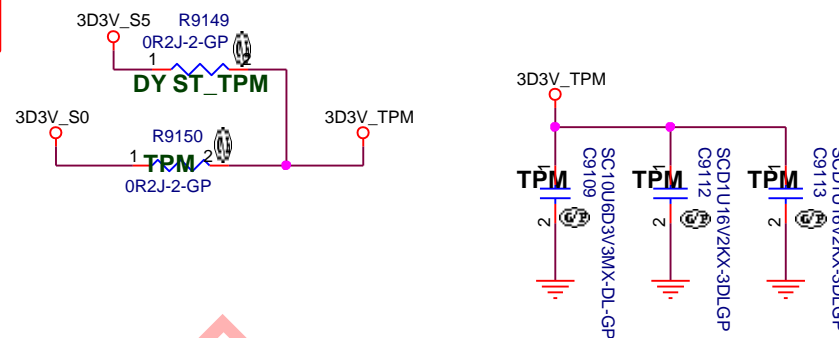
Byte 7	56~63
Byte 6	48~55
Byte 5	40~47
Byte 4	32~39



Main Func = TPM

Eletro-XTechnical

[7,40,61,62,63,66,76] PLT_RST# >>> _____
[18,24,25] SPI_CLK_ROM >>> _____
[15,18,24,25] SPI_SI_ROM >>> _____
[18,24,25] SPI_SO_ROM >>> _____
[18] SPI_CS_ROM_N2 >>> _____
[20] PIRQA# >>> _____
[18] TPM_SPI_IRQ# >>> _____



<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (TPM)

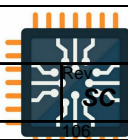
Size
A4

Document Number

Mockingbird CML

Date: Monday, December 09, 2019

Sheet 91 of



Firmware SW

ME_FWP 2 R9806 1 ME_FWP_SW

0R0402-PAD

SA 1026

MESW1

SW-SLIDE3P-1T-GP

ME_FWP 3

ME_FWP_SW 2

R9801

MESW1 1

3D3V_S5_PCH 2

1KR2J-1-GP

MESW

NP2

NP1

62.40018.641

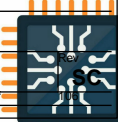
R9802

4K7R2F-GK

SA 1026

	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override



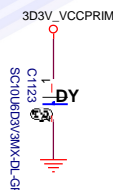
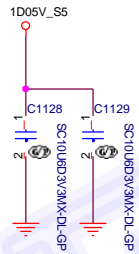
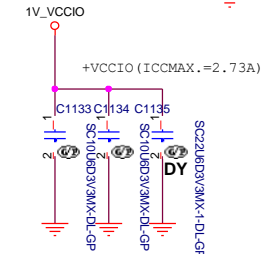
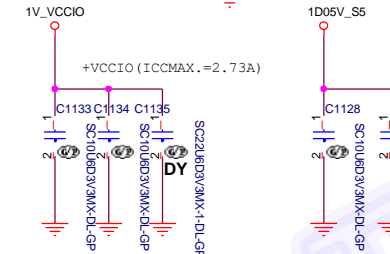
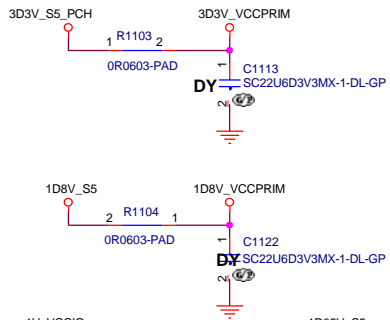
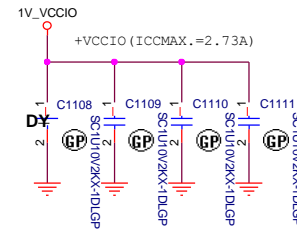
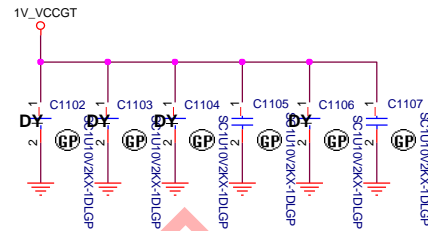
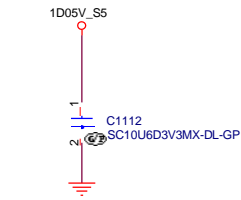
SSID = CPU

PCH DERIVED RAILS

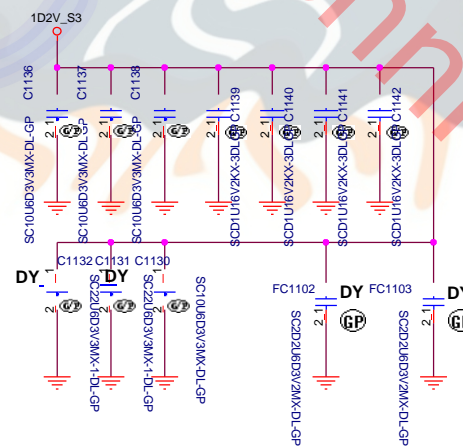
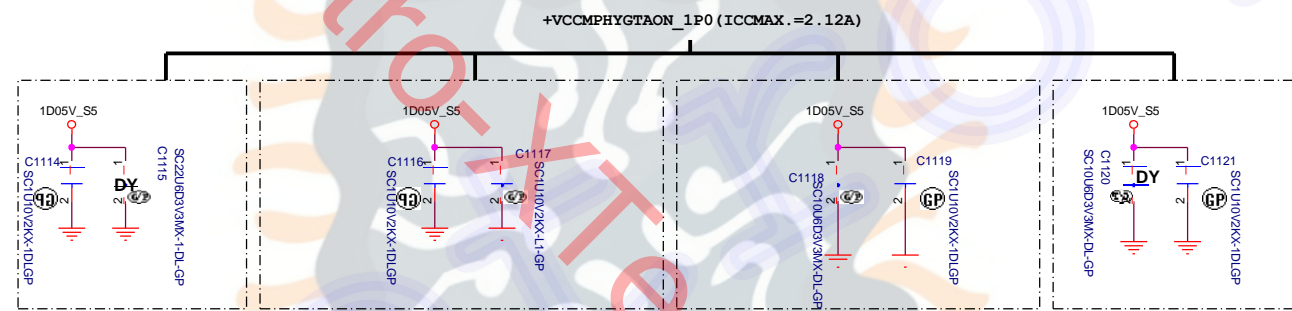
UNSLICED GT

VCCIO

Eletr-XTechnical



U-line 23e 28W
IccMax current-10ms max = 34 A

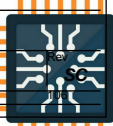


Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,
Taipei-Hsien 221, Taiwan, R.O.C.

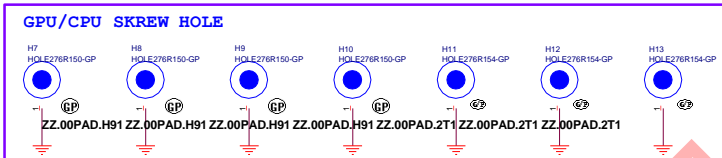
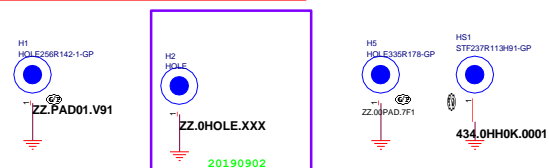
Title: CPU (Power CAP2)
Size: A3 Document Number: Mockingbird CML
Date: Monday, December 09, 2019 Sheet: 11 of 11



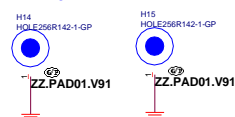
Eletr-X

Eletr-XTechnical

5
Main Func = UnusedParts



TYPEC SKREW HOLE

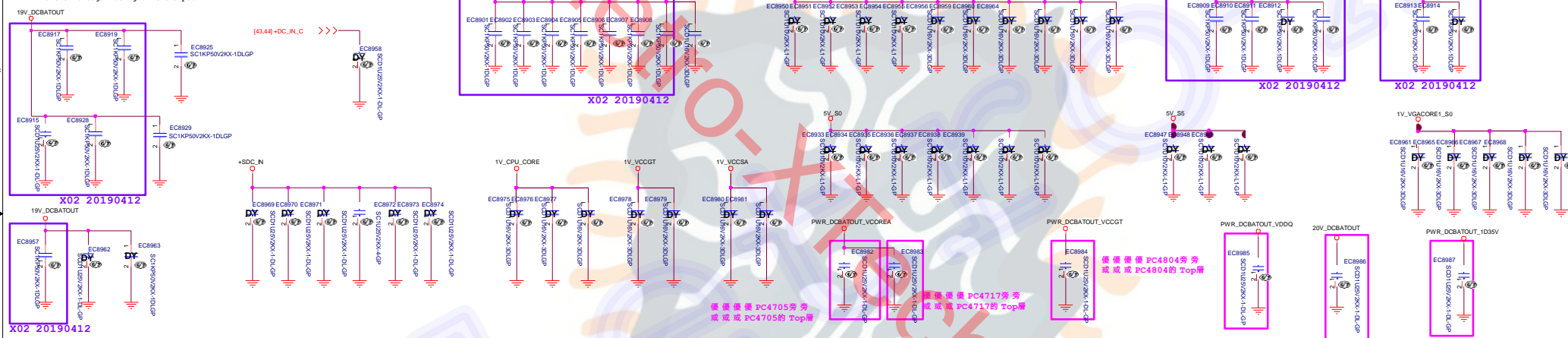


HDMI SKREW HOLE

For acoustic noise

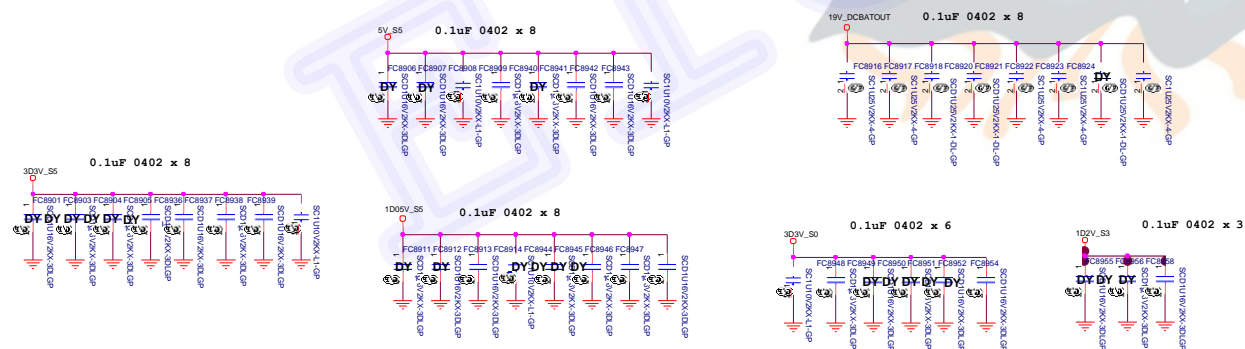
Main Func = EMI Capacitors

Mind the voltage rating of the caps.



Main Func = RF Capacitors

Mind the voltage rating of the caps.



«Come Design»

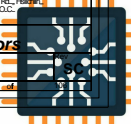


Wistron Corporation
2/F, 88, Sec. 4, Huifeng Rd., PM, Hsinchu, Taiwan

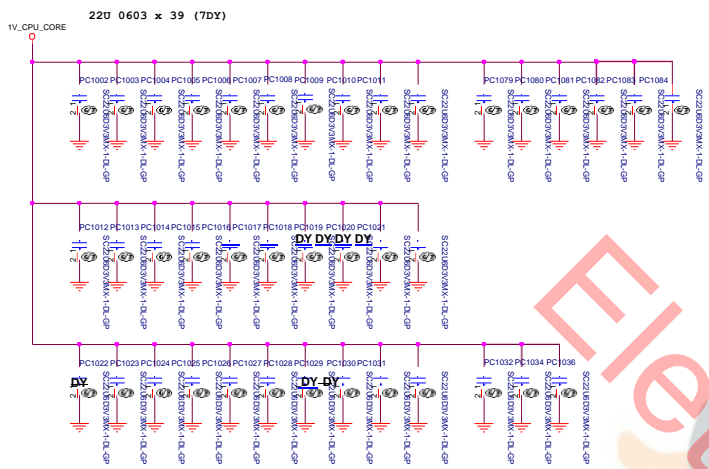
UNUSED PARTS/EMI Capacitors

Size Document Number	Mockingbird CML		
A2			
Date: Monday, December 09, 2019	Sheet		

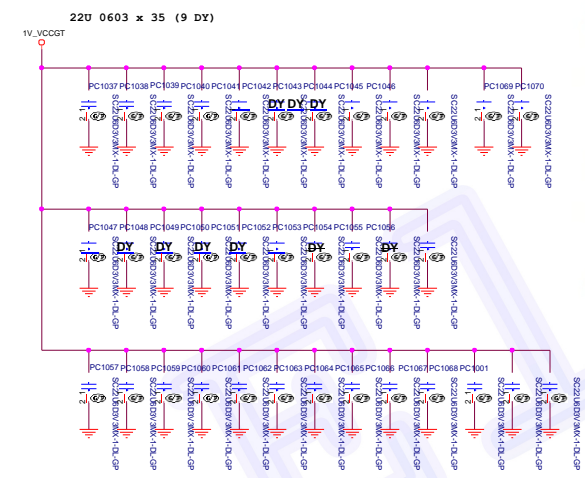
Eletro-X



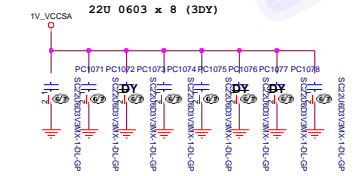
1V_CPU_CORE



VCCGT



VCCSA



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	Place as close to the package as possible
	8x 10uF 0402		
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCGT	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
VCCSA		4x 0402	Placeholder only.
	6x 10uF 0402	7x 10uF 0402	
	2x 47uF 0805 (6.3V)		
	2x 0805		Placeholder Only
VDDQ		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
VCCIO	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		Placeholder Only
VCCPLL_OC	1x 1uF 0402		Do not merge VCCPLL, VCCPLL_OC and VCCGT to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		Placeholder Only.
			Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		
VCCGTB	1x 1uF 0402		

Notes:

- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR.
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

<Core Design>

Wistron Corporation

2/F, 88, Sec. 1, Hsin-Tai Wu Rd., Taipei 100, Taiwan, R.O.C.

Tel: +886 (0)2 2711 2211

Size: 100mm x 100mm

Document Number: A1

Date: Monday, December 18, 2018

Printed: 10

CPU(CORE Power Cap)

Mockingbird CML

